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A Real-time High Reliable Multi-chip Transmission Technology

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Abstract. In this paper, a LVDS parallel data re-calibration circuit for network interconnection on multi-chip is proposed. The operation states of the re-calibration circuit can be divided into four states: normal, empty, calibration and recovery. In each state, normal data packets that require cross chip transmission have different routing methods. During the operation of re-calibration circuit, normal data packets that need to be transmitted across chips can be routed to the destination bare chip through the bypass output channel using integrated routing algorithm. By using the ingenious isolation mechanism, not only normal data packets can be avoided to be lost, but also test data packets can be prevented from flowing into non calibrated circuit modules. So, it can ensure the normal operation of the integrated network. The re-calibration circuit proposed in this paper can enhance the reliability of multi-chip network interconnect system in real time, and has no significant impact on the system performance.

Keywords: multi-chip network, LVDS, calibration circuit, isolation mechanism.

1. Background

In the context of high-performance computing and big data applications, system architects need to constantly integrate more cores, accelerators, and memory within given power range. With the development of integrated circuit technology into the post-Moore era, electronic and physical limitations make it more and more difficult to continuously upgrade the advanced semiconductor fabrication. Continuing to implement large systems through single chips is bound to face problems such as greatly reduced yield and sharply increased design and mask costs. The traditional single-chip design scheme is changed into multi-chip design, and the use of high-speed interface for interconnection or advanced packaging technology becomes a better choice[1-2]. LVDS (Low Voltage Differential Signaling) is a low-swing differential signaling technology that has the advantages of low power consumption, low bit error rate, low cross talk, and low radiation[3-4]. So it can meet the requirements of high-speed interconnection across bare cores.

Physical factors such as chip wear and environmental change may cause circuit-level faults in inter-chip interconnect components. For example, aging may increase the transmission delay of inter-chip links, and lead to errors in parallel data sampling between chips. Temperature change may also cause waveform of voltage and current, and lead to errors of logical signal. These faults will further lead to data packet structure errors in cross-chip transmission or even loss of microchips or packets, which will seriously affect the operation and performance of the inter-chip integrated network [5-7]. If physical fault can be detected during the period between occurrence of a physical fault and the cause of a network-level fault, fault tolerance mechanisms such as appropriate routing algorithms or redundancy techniques can be applied to prevent network-level fault.

Fault detection and diagnosis are the prerequisite to activate fault tolerance mechanism. Previous fault-tolerance techniques for LVDS interconnect between multi-chip networks have relied mainly on off-line testing mechanisms. Due to the difficulty of creating corresponding operating conditions in dynamic environments and designing appropriate testing mechanisms, offline testing is almost impossible to detect faults caused by environmental conditions such as temperature, voltage drop, and aging. In order to enhance

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the reliability of the cross-chip interconnect of multi-chip network in real time, this paper proposes an inter-chip LVDS parallel data calibration circuit, which helps to detect and diagnose faults as early as possible and allows corresponding measures to be taken later[8-10].

2. The Proposed Architecture

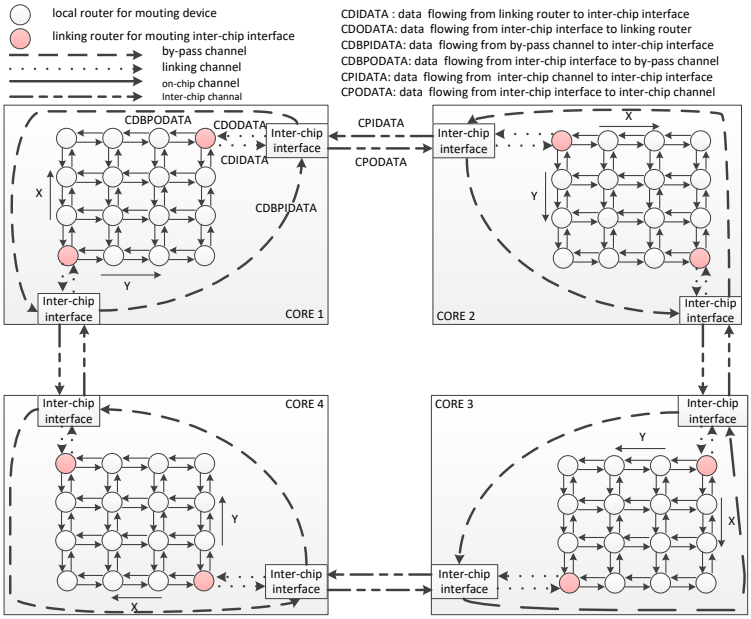

Fig. 1: Structure diagram of multi on-chip network cross chip interconnection system

The structure of multi-chip network cross-chip interconnection system is shown in Fig. 1 [11-13]. In this paper, the parallel LVDS data calibration circuit for network interconnection on multi-chip is proposed. The circuit can control the affected packets in the process of inter-chip interconnection from normal state to calibration state or from calibration state to normal state. It can minimize the probability of packet blocking in cross-chip transmission and ensure the smooth transmission of packets[14-15].

The commonly used calibration algorithms currently include Feed Forward Equalizer (FFE) and Forward Error Correction (FEC). FFE filters out noise in specific frequency bands by adjusting the weights of different bits. In the process of high-speed data transmission, FFE is needed to enhance the high-frequency component and improve the transmission quality of the signal. FEC technology adds redundant error correction codes to the transmission code column to resist interference caused by the channel and improve the reliability of communication system.

The parallel calibration algorithm circuit proposed in this paper is different from the above two algorithms. It is designed for the scenario of multi-channel signal parallel transmission, where one channel is transmitted as a clock signal. In order to achieve real-time calibration of parallel channels, the calibration algorithm circuit first adjusts the clock delay to obtain the optimal delay point for channels, and then adjusts the data delay to verify the failed channel.

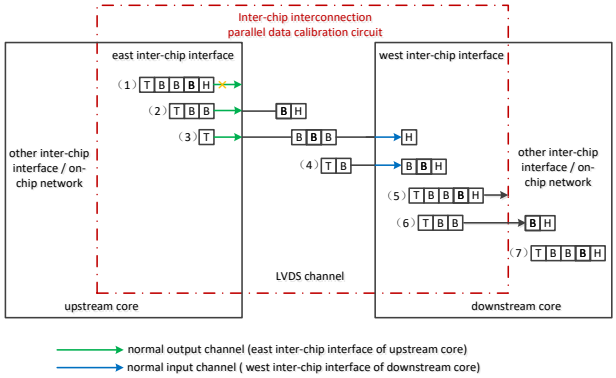

Fig. 2: Inter-chip interconnection emptying state

As shown in Fig. 2, before the inter-chip interconnect LVDS link is calibrated, there is a transition stage from the normal state to the calibration state, which is as known as the emptying state. At this stage, the indirect port on the east side of the upstream bare core will stop sending new normal data packets to the indirect port on the west side of the downstream bare core through the normal output channel (Case 1), but it continue sending all partially transmitted normal data packets through the normal output channel (Case 2-3).The normal input channel of the indirect port on the west side of the downstream bare core needs to fully receive the normal data packets transmitted across the chip at this stage (Case 2-4). However, the data packet shown in case 5-7 has entered the normal input channel buffer of the indirect port on the west side of the downstream bare core, so it is not affected by the transition phase. Once the normal packets of the area involved in the inter-chip interconnect LVDS channel are emptied, the calibration state can be officially entered.

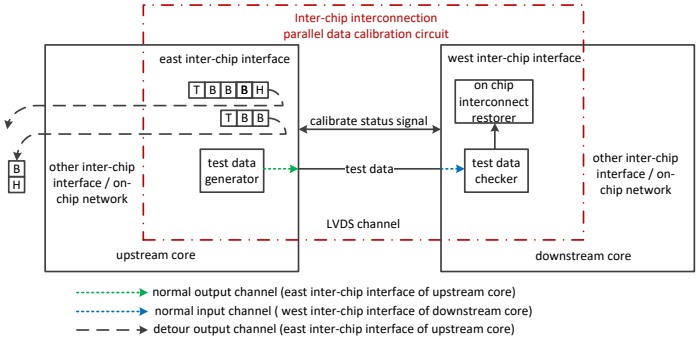

Fig. 3: Inter-chip interconnection calibration status

As shown in Fig. 3, when the inter-chip interconnection is in the calibration state, the LVDS channel between the upstream bare core east chip indirect port and the downstream bare core west chip indirect port will only be used to transmit the calibration state signal and test data required for calibration. The upstream bare-core test data generator generates test data that highlights LVDS link failure or alignment. This test data is connected to its LVDS channel by using the test output channel of the east chip indirect port. The test data transmitted by LVDS channel will enter the test data checker through the test input channel of the indirect port on the west side of the downstream bare core. The test data checker will judge the transmission status of LVDS link by sampling test data. The inter-chip interconnect restorer adjusts the delay or transmission scheme of each channel of LVDS according to the inspection result of the test data checker. The normal data packets that need to be transmitted across chips can be transmitted to their destination bare core by detour output channel using the integrated adaptive routing algorithm between chips.

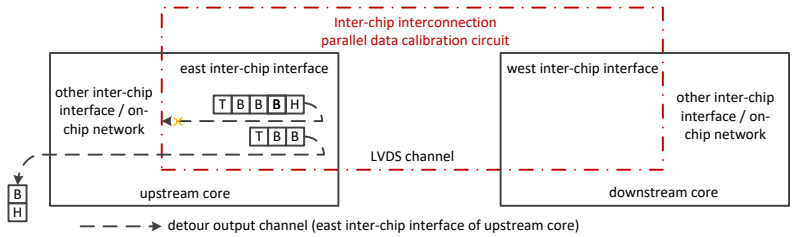

Fig. 4: Inter-chip interconnection recovery status

As shown in Fig. 4, when the inter-slice interconnect calibration is done, there is also a transition stage from the calibration state to the normal state, which is called the recovery state. In this state, the indirect port on the east side of the upstream bare core will stop sending new normal packets through the detour output channel, but it will continue to bypass and send normal packets that have already been partially transmitted. Once the normal data packets that need to be sent using the detour output channel are cleared, the normal state can be restored.

When the inter-chip interconnection is in the normal state, the east chip indirect port of the upstream bare core will not use the detour method to route the normal data packets that need to be transmitted across the chip. Normal data packets are routed to the upstream bare core west chip indirect port through the normal

output channel of the upstream bare core, and then enter the on-chip network or other chip indirect ports of the downstream bare core through the normal input channel.

3. System Realization

In this paper, an LVDS parallel data automatic calibration circuit for cross-chip interconnection is proposed. Fig. 5 shows the structure diagram of the automatic calibration circuit. The circuit consists of two parts, which are distributed in the transmitter of the upstream bare core and the receiver of the downstream bare core. In practical application, the indirect port of each bare core has the function of receiving and sending at the same time, so it also has its own corresponding calibration circuit module, which belongs to two sets of calibration circuits respectively. When a single bare core acts as receiver and transmitter, the calibration circuit can work independently, but it needs to cooperate with the sending or receiving of another bare core to build a complete calibration system.

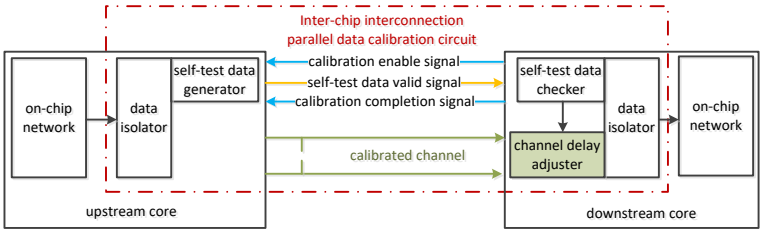

Fig. 5: Parallel data automatic calibration circuit structure

The automatic calibration circuit mainly consists of data isolator and self-checking data generator which located in the upstream bare-core sending terminal, and data isolator, self-checking data detector and channel delay regulator which located in the downstream bare-core receiving terminal. The status of calibration ENABLE signal and calibration COMPLETE signal are generated at the receiver and transmitted to the sender by LVDS link. The operation status of the whole calibration circuit is controlled by these two signals. When the calibration ENABLE signal is high and the calibration COMPLETE signal is low, it means that the signal transmission channel across chips is under calibration.

The self-check data generator generates self-check data in a certain format in the calibration state and sets the ENABLE of self-check data to 1.The ENABLE of self-check data is also transmitted to the receiver of the downstream bare core through the LVDS channel together with the self-check parallel data. The self-checking data checker compares the valid self-checking parallel data received over a period of time with the known self-checking data to determine which channels are not properly sampled, and then submits the channel alignment information to the channel delay adjuster. The channel delay adjuster will adjust the delay of the clock channel and the data channel according to the set calibration algorithm. After the adjustment delay of each channel is stabilized, the self-check data checker will receive the self-check data again for a period and make the corresponding judgment. If there are still data channels out of alignment, it needs to continue to adjust the clock or the data channel delay. The function of the data isolator is to choose whether to suspend the transmission of normal data packets between bare cores according to the calibration state. During calibration, the data isolator of the transmitter will prevent intra-chip data packets from being transmitted to inter-chip links， which aims to prevent the loss of normal packets and avoid interference in the calibration process. A data isolator is also deployed at the receiver to prevent the self-checking data received by the downstream bare core from flowing into the chip and affecting the normal operation of the network on the chip.

4. The Workflow and Test

Fig.6 is a schematic diagram of the whole process of the calibration circuit, which will be explained in detail as fellow.

To solve the problem of cross-chip transmission error caused by time sequence difference between channels, the existing adjustment method is mainly to preset the delay value for each channel. After observing the sampling results of each channel through continuous experiments, the delay value of each channel is repeatedly corrected. The static preset debugging method is time-consuming and low precision. In

this paper, through the hardware circuit to realize the detection and automatic repair of the alignment of each channel, saving manpower and time resources, also achieving a better calibration performance.

To enhance the calibration efficiency and precision of cross-chip transmission, this paper proposes a novel approach that utilizes hardware circuits to automate the detection and repair of channel alignment. By incorporating intelligent components into the circuit design, we aim to eliminate the need for manual presetting and repetitive corrections. Instead, the system will dynamically monitor the sampling results of each channel, and automatically adjust the delay values accordingly.

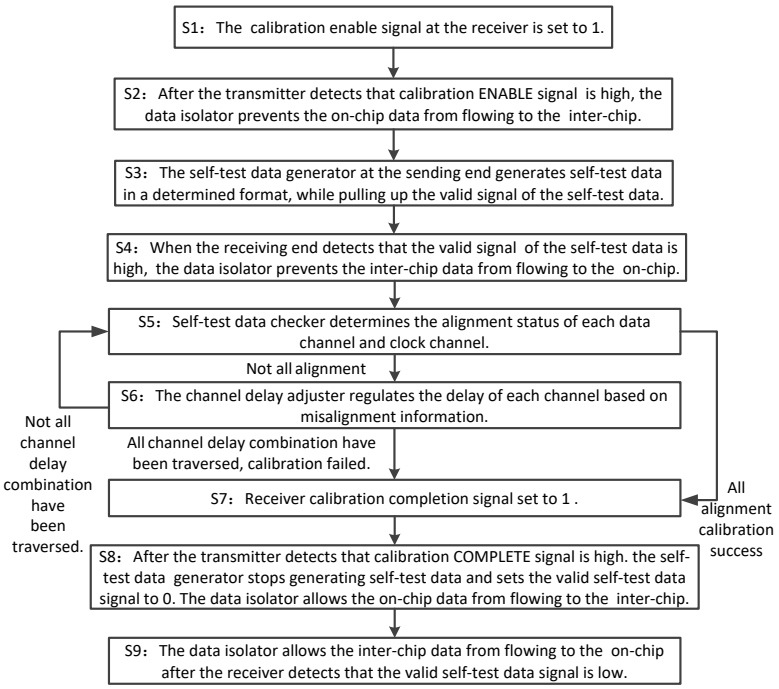

Fig. 6: Automatic calibration circuit operation process state diagram

The simulation environment is as follows: the right receiver of the upstream bare core is set to the unaligned initial state to prepare for the subsequent verification of the automatic calibration function.Due to the increased delay of the data channel, the problem of non-alignment occurs when the data is transmitted. The simulation figure is shown in Fig. 7.

By the graph, it shows that CPCLK_ERX clock should collect low-level at its rising edge, but the path delay of lane48, 60, 66, 72, 54 causes the collected data to be misaligned and result is high-level. Therefore, the data needs to be processed.

When the calibration signals - **autocalib_good_erx** and **autocalib_over_erx** are both 1, the calibration is complete, which means all data channels are aligned (0 at clock rising edge).

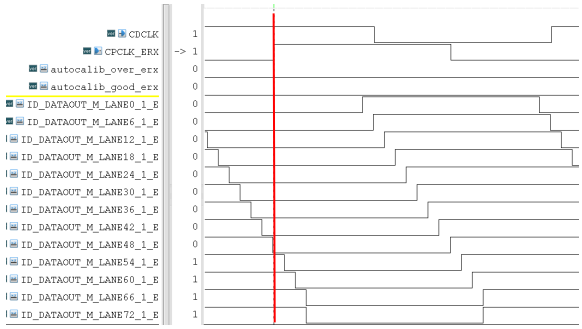

Fig. 7: Waveform plot before calibration

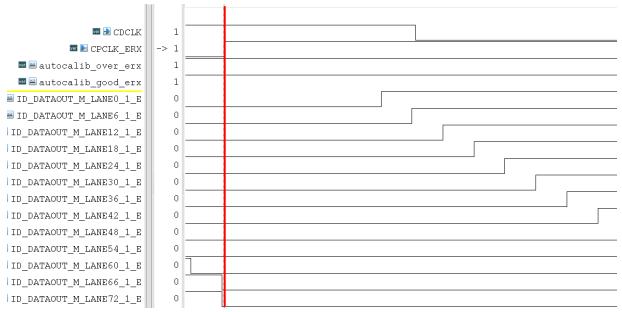

Fig. 8: Waveform plot after calibration

The Fig.8 shows that after the calibration data is collected at rise edge as low level, show that calibration data is completed. To ensure that the calibration circuit does not affect the normal data path in practical applications, a data isolation circuit is added to realize the analysis of calibration data and normal data.

Transmitter data isolation is shown in Fig. 9. The auto-calibration enabling signal **encalibra_etx** of the east port of the upstream bare core is 1 and the auto-calibration process ending signal **calibra_over_etx** is 0, indicating that the auto-calibration process is in progress.

CALIB_DATA_ETX is the self-check data generated by automatic calibration. **CALIB_CPOVALID_ETX** is the enabling signal of self-check data. **CPODATA_E_reg1** represents the output data of the network on-chip. **CPOVALID_E_reg1** is the enabling signal for the output data of the network on chip. **OD_IDATAIN_M_LANE*_0_E** is the input signal of the LVDS channel.

As is shown in waveform diagram, during the calibration process, the input signal of LVDS channel is always the self-check data **CALIB_DATA_ETX** generated by automatic calibration, and the output data of network on-chip does not flow to the inter-chip link.

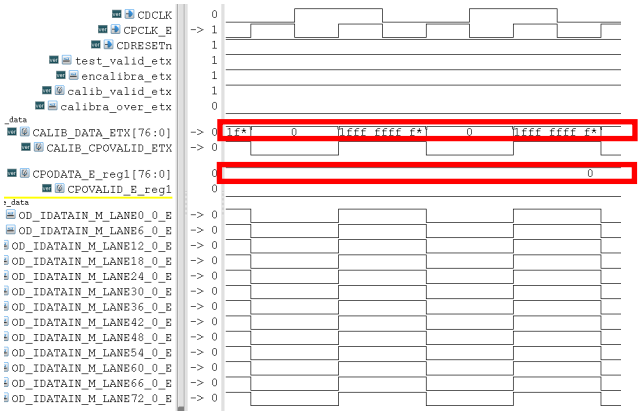

Fig. 9: Data waveform of the upstream transmitter

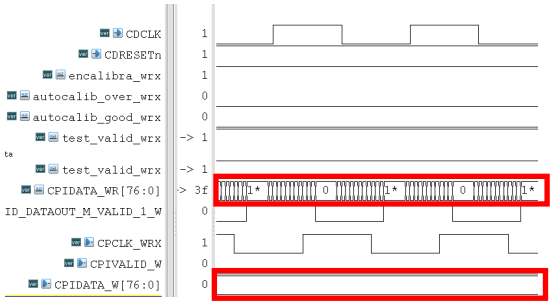

Fig. 10: Waveform of downstream receiver data

Receiver data isolation is shown in Fig. 10. The auto-calibration enabling signal **encalibra_wrx** at the west port of the downstream bare core is 1, and the **autocalib_over_wrx** at the end of the calibration process is 0, indicating that the auto calibration process is in progress.

CPIDATA_WR indicates the self-check data received from the west interface of the downstream bare core. **ID_DATAOUT_M_VALID_1_W** indicates that the self-check data is received. **CPIDATA_W** is the input data of the network on chip. **CPIVALID_W** is an enabling signal for the input data of the network on chip. **test_valid_wrx** = 1 means that the self-check data received at the west end of the downstream bare core is enable. According to the waveform diagram, the self-check data received at the west port of the downstream bare core was not input into the network on-chip during the calibration process.

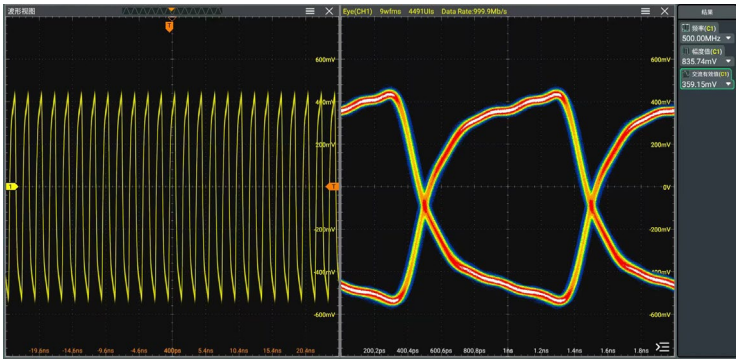

Fig. 11: Eye diagram after Tape-out test

After Tape-out, the signal quality of LVDS was tested. From the LVDS eye diagram, the effective AC differential amplitude was about 359.15mV, and the rise and fall time of 20% to 80% was about 300ps, meeting the parameter requirement of IEEE LVDS standard.

5. Summary

The LVDS parallel data calibration circuit proposed in this paper can diagnose and recover faults of cross-chip interconnect circuits and can enhance the reliability of cross-chip interconnect of multi-chip

networks in real time. In addition, the normal data packets that need to be transmitted across chips during the operation of the calibration circuit can also be routed to the destination bare core through the detour output channel using the integrated routing algorithm between chips. This mechanism greatly reduces the blocking probability and time of normal data packets, and avoids the operation of calibration circuit causing great influence on the performance of network on multi-chip interconnection system.

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7. References

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