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Verification Platform of 40Gbps High-speed Serial Interface Chip Based on UVM

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Abstract. This paper proposes a verification platform based on UVM for a 40Gbps high-speed serial interface chip. Using the platform as basis, both the RTL codes and the relevant netlist after synthesis of the 40Gbps chip are fully tested to ensure the correctness of the chip's functions. This guarantees the success of the chip's tap-out.

Keywords: UVM, High-speed Serial Interface Chip, 40Gbps, Verification Platform.

1. Introduction

As chip size increases, the development and verification cycles of chip lengthens. According to empirical analysis, the proportion of design and function verification is approximately 3:7 at the digital chip design process [1]. During chip design, problems found later can bring more serious damage. Therefore, if complete functional verification can be conducted and functional defects of design can be discovered at the RTL period, the loss during the development can be minimized. Considering the modern integrated circuit (IC) common in the IMEEM era, the time consumption and workload of function verification are especially large. Therefore, how to reduce the verification time and ensure the quality and efficiency of verification are hot issues that should be considered carefully by each IC design company.

Verification methodologies emerge to solve a series of problems confronted during verification, such as the complexity and completeness of verification. Since 2000, Synopsys, Mentor, and other corporate behemoths have launched their own verification methodologies. The derivatization process of verification methodology is illustrated in Figure 1. The figure shows that after a period of coexistence with various methodologies, chip verification methodologies are unified into a new generation of verification methodology, that is, universal verification methodology (UVM) launched by Cadence, Mentor, and Synopsys [2][3]. At present, UVM is the most popular verification methodology, and it is promoted by all major EDA manufacturers. UVM draws essence from many verification methodologies, including AVM, OVM, and VMM, thus representing up-to-date progress of verification technology. The verification process is greatly simplified by the widespread application of UVM.

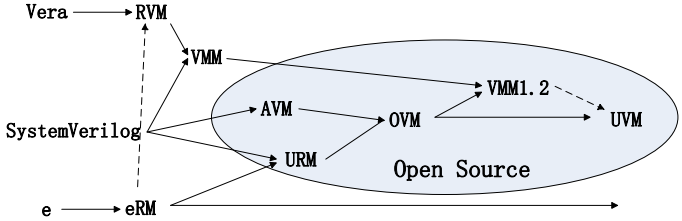

Fig. 1: The derivatization process of verification methodology

In this paper, we proposes a verification platform for a 40Gbps high-speed serial interface chip, on the

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basis of UVM. Using the platform, a complete verification is conducted to ensure the success of the chip's tap-out.

2. Introduction of the Verification Object

The verification object is a 40Gbps high-speed serial interface chip. Figure 2 illustrates the overall structure of the chip. The top layer includes six modules: CCU, RESET, RM, TST, NP, and HSS modules. CCU and RESET provide global clock and reset signal. RM contains I2C interface and register access chain. TST generates pseudo-random binary sequence (PRBS) and user defined data for the high-speed serial interface. NP contains two submodules: LLP link layer and PCSFEC coding layer. LLP is in charge of link initialization and handshaking functions, and PCSFEC is in charge of data encoding, decoding, error correction and parallel binding functions. HSS module contains variable speed control, power management, BIST-1lane self-testing with adaptive equalization, and PHY module.

The 40Gbps chip supports two connection topologies: single chip loopback via cable line and dual chip direct data transmission. In each connection mode, two working modes are supported: PRBS random number message transmission and user-defined data (user_data) transmission. Besides, the chip supports such functions as continuous transmission after lane down, lane polarity inversion, and lane out-of-order connection and so on. In terms of verification, there are many combinations among the connection mode, working mode and function points. Therefore, it is difficult to meet verification requirements by using traditional hardware description languages. This paper adopts the systemverilog-based [4] UVM as the basis to construct the verification platform. UVM provides abundant object-oriented class hierarchy structures, and introduces staged execution, callback, and report mechanisms which greatly simplify the construction of verification platform and improves the verification efficiency.

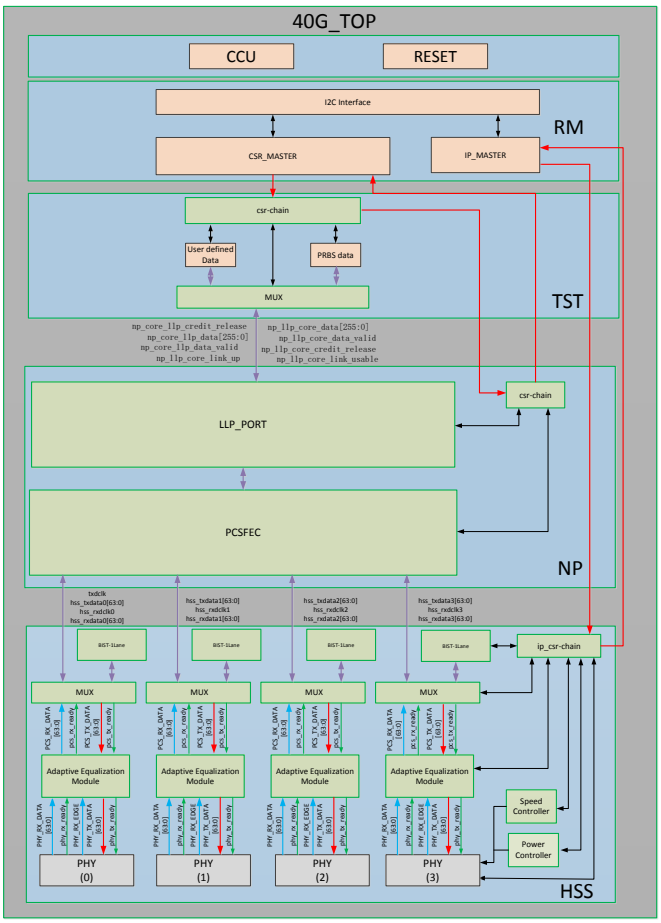

Fig. 2: Overall structure of the 40Gbps high-speed serial interface chip

3. Verification Platform Based on UVM

Figure 3 presents the overall framework of the verification platform we proposed. It contains 10

submodules: “driver,” “monitor,” “sequencer,” “sequence,” “agent,” “reference_model,” “score_board,” “reset,” “config,” and “iic_driver.”

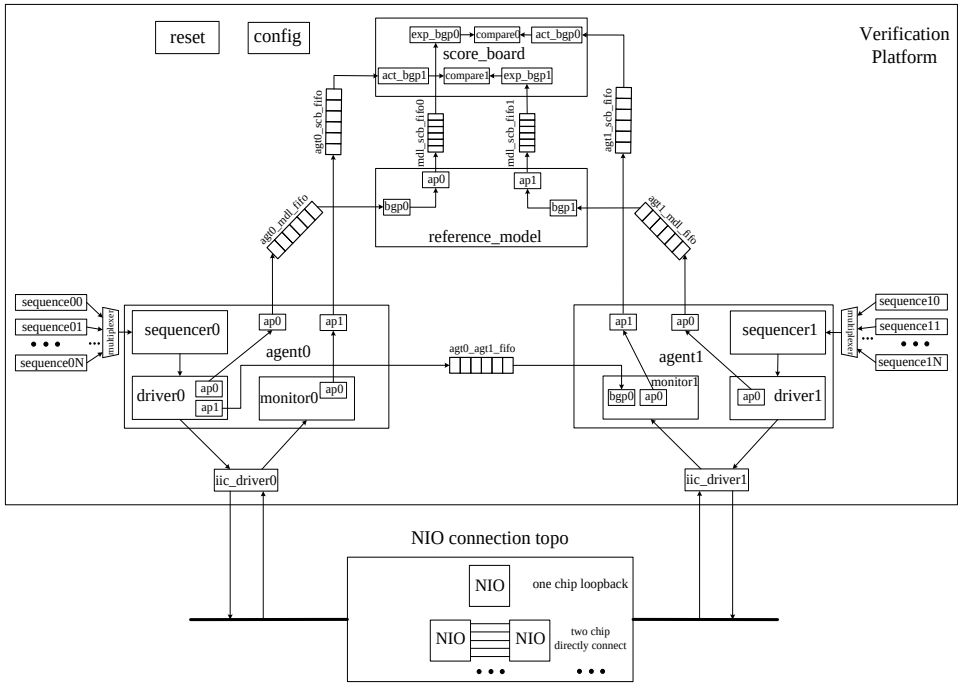

Fig. 3: Overall framework of the verification platform

The main tasks of “driver” include 1) obtaining test incentives from “sequence” and sending them to DUT (via “iic_driver”) and “reference_model”, respectively, 2) sending various configuration commands to DUT according to configuration information of “config” module, and 3) flow controlling during the packets transmission process. Submodule “monitor” is in charge of monitoring results returned from DUT and forwarding them to “score_board”. Submodule “sequencer” works together with “sequence,” which is responsible for providing “driver” with specific test incentives (e.g., various random packets and fixed packets with specific meaning). One “sequence” is responsible to generate a specific type of packet, and “sequencer” decides which sequence packet to send to “driver” based on the current configuration information. Submodule “agent” is the container of “driver,” “monitor,” and “sequencer.” Typically, “agent” corresponds to physical interface protocol, and different interface protocols correspond to different “agents.” Interface protocol sets up the data exchange format and modalities, and “agent” achieves this substance of the interface protocol via “driver” and “monitor.” Our 40Gbps chip verification platform includes two sets of identical “agents,” which are responsible for data sending/receiving of two connected 40Gbps chips. Submodule “reference_model” is the reference model that is a fully functional equivalent of DUT. After the test incentives passes the “reference_model,” the expected output of DUT can be obtained, and then “scoreboard” compares these outputs with DUT to verify the correctness of DUT’s functions. On the 40 Gbps verification platform, “reference_model” is such easy that test packets from “driver” only need to be intact (or inject errors as needed) to be sent to “score_board.” Submodule “score_board” receives result packets from DUT via “monitor” and test packets from “driver,” and it compares the two packets to confirm whether DUT is running normally. Submodule “reset” is in charge of reset operations for DUT. Submodule “config” is a kind of profile, and the functions implemented by the whole verification platform can be set and restructured by simply configuring this submodule. Currently, supported configuration information includes the following: 1) Whether EEPROM is configured online. 2) Whether external I2C controller is configured online. 3) The connection topology of 40Gbps chip is currently configured to support single chip loopback and double chip direct connection with two kinds of topology. 4) The transmission mode of chip is presently configured to support two modes: PRBS random packet transmission and user defined data. 5) Configure on/off and various function point tests (e.g., register access, fault injection testing or lanes out-of-order connection testing). 6) Configure simulated verification environment (ASIC or FPGA). 7) Whether the simulated chip is configured to set single Lane or 4-Lane. 8) Configure the platform to execute netlist-level or RTL code simulations.

Each module exchanges data via various TLM transmission ports provided by UVM (e.g., uvm_actual_port(ap) and uvm_blocking_get_port(bgp)) and FIFOs.

The 40Gbps chip verification platform features the following main characteristics:

1. Good maintainability and extensibility. On the platform, all modules assume clear division of work, and locating the related module to revise according to the test requirements is easy. For example, if the task of test packet generation is assigned to sequencer/sequence, then "drive" will only be in charge of data transmission, without focusing on data generation. If the test packet format needs to be revised or a new packet format must be added, then it only needs to revise or add new "sequence" with other modules unchanged.
2. Configurability. The platform exhibits good configurability. By simply adjusting the configure profile, the verification platform can be customized to execute different test cases.

4. Results

4.1. Verification Results

The structure illustrated in Figure 3 is implemented using the simulation tool vcs E-2011.03-SP1_Full64 of Synopsys company [5]. Using the platform as basis, the RTL code as well as corresponding netlist of 40Gbps chip are completely tested.

Figure 5 shows the scoreboard log of transmitting user defined packets when configured as double chip direct connection mode. The "score_board" receives two packets, expected value from the "reference_model" and the other is the actual packet received. If the two packets have the same content, which indicates the communication is considered to be successful.

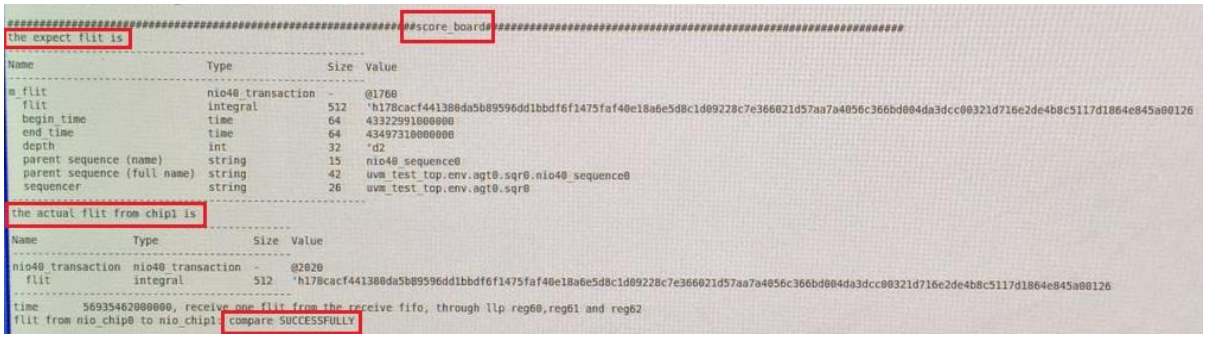

Fig. 5: the score_board log when transmitting user defined packets

Figure 6 shows a part of the simulation results when the environment is configured to transmit PRBS random packets in single chip loopback mode. One can see that only flit_right_count increased, which demonstrates the PRBS packets are transmitting correctly.

Fig. 6: the waveform of transmitting PRBS random packets in single chip loopback mode

Table 1: random tests results (RTL & netlist & netlist with SDF)

Connection mode	Transmission mode	Object	# of Packets transmitted	result
Single chip loopback	PRBS	ASIC	10^{10}	pass
		FPGA	10^{10}	pass
	User defined data	ASIC	20480	pass
		FPGA	20480	pass
double chip direct connection	PRBS	ASIC	10^{10}	pass
		FPGA	10^{10}	pass
	User defined data	ASIC	20480	pass
		FPGA	20480	pass

Tables 1 and 2 provide the random and partial function point testing results, respectively. Each test is conducted for both ASIC and FPGA.

Table 2: partial function point test results (RTL & netlist)

Test Function Point	Object	result
PCS/PHY wrapback	ASIC	pass
	FPGA	pass
Tx/Rx lane polarity inversion	ASIC	pass
	FPGA	pass
PRBS with PCS closed	ASIC	pass
	FPGA	pass
continuous transmission after lane down	ASIC	pass
	FPGA	pass
PHY BIST (prbs7/11/31）	ASIC	pass
	FPGA	pass
Registers access	ASIC	pass
	FPGA	pass
Errors inject	ASIC	pass
	FPGA	pass
Lane out-of-order connection	ASIC	pass
	FPGA	pass

4.2. Testing Results of the Chip

The 40Gbps chip is manufactured using the TSMC 65nm technology. After RESPIN, we build a PCB testing board and based on it, the chip is tested completely (the test environment is shown Figure 7). Test results show that all the functional and performance criteria of the chip meets the expected requirements (e.g., the eye diagram of transmission of PRBS7 under 40Gbps rate is shown in the figure 8), which indicates that the verification platform successfully ensure the correctness of chip's functions as well as the successful tap-out of the chip.

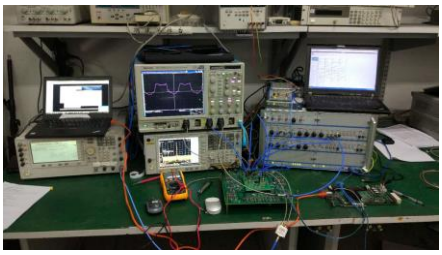

Fig. 7: the test environment of the 40Gbps chip

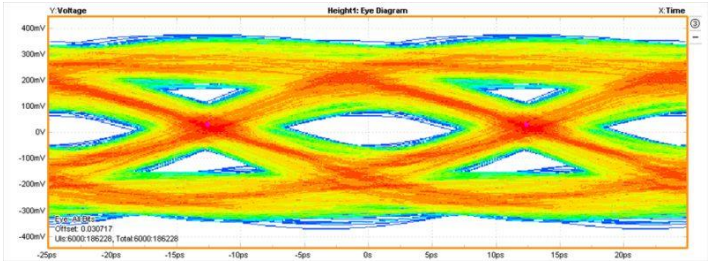

Fig. 8: the eye diagram of transmission of PRBS7under 40Gbps

5. Conclusion

Through our study, we demonstrated that our proposed UVM based verification platform for the 40Gbps high-speed serial interface chip had good maintainability and extensibility. The success of the chip's tap-out is ensured using this platform. This work was supported by the National Natural Science Foundation of China under Grant 61502507.

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