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A CMOS Temperature Sensor with an Inaccuracy of 0.5℃ from -20℃ to 80℃

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Abstract: A smart temperature sensor is designed for very large scale integration (VLSI) systems to control power and temperature. PNP transistors are designed as sensing elements to generate temperature dependent output voltage. Three main techniques to enhance the accuracy are described as following: a chopped current gain independent bias circuit, dynamic element matching (DEM) and curvature compensation. To reduce area and power consumption, successive approximation register (SAR) ADC with split capacitor DAC structure is used, which achieves an effective number of bits (ENOB) of 10.4 bits after simulation. The sensor is designed in a TSMC 0.18μm 1P6M standard CMOS technology and consumes 700uA under a supply voltage of 1.8V. The proposed sensor is capable of working in the temperature range of -20 ℃ ~ 80 ℃. With the one-point calibration, the sensor shows an inaccuracy of 0.5 ℃.

Keywords: temperature sensor, dynamic element matching, SAR ADC, offset cancellation

1. Introduction

Temperature sensors are widely used in our daily life. The sensor designed in this paper can be integrated into VLSI system to provide safe, controllable and even personalized real-time online monitoring. It can be used in mobile terminal, industrial system, building control system and home intelligent facilities.

In this paper, a temperature sensor based on the characteristics of triode is designed. It uses independent bias circuit to eliminate the current gain of triode, curvature correction technique to improve the linearity and dynamic element matching (DEM) to reduce the errors from mismatch of current mirrors. Furthermore, SAR ADC with split capacitor DAC structure is employed to achieve a more ideal result [1]-[4].

2. Topological Structure

The principle diagram of the sensor is shown in Fig.1. To get a real-time temperature consequence, a ratio-metric measurement has been taken into consideration.

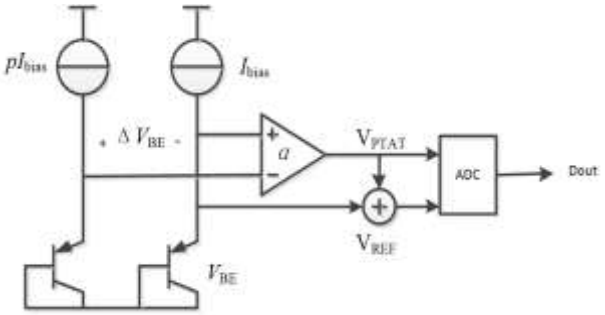

Fig. 1: Principle diagram of the temperature sensor.

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A pair of matched diode-connected substrate PNP bipolar transistors flows through different currents with ratio p to generate V_{BE} and ΔV_{BE}. ΔV_{BE} is a proportional to absolute temperature (PTAT) voltage. V_{BE} and ΔV_{BE} can be approximated as:

$$V_{BE} \approx \frac{kT}{q} ln\left(\frac{I_{bias}}{I_S}\right) \tag{1}$$

$$\Delta V_{BE} = \frac{kT}{q} ln\left(\frac{pI_{bias}}{I_S}\right) - \frac{kT}{q} ln\left(\frac{I_{bias}}{I_S}\right) = \frac{kT}{q} ln\, p \tag{2}$$

where k is the Boltzmann's constant, T is the absolute temperature, q is the electron charge, I_{bias} is the collector current and I_{S} is the saturation current of the transistor.

A bandgap reference voltage V_{REF} can be produced with V_{BE} and ΔV_{BE}.

$$V_{REF} = V_{BE} + \alpha \Delta V_{BE} \tag{3}$$

A PTAT output μ can be generated as following [5]:

$$\mu = \frac{\alpha \Delta V_{BE}}{V_{REF}} \tag{4}$$

The real Celsius temperature is be obtained by quantization, where $\mathrm{A} \approx 600, \mathrm{B} \approx -273$:

$$D_{out} = A \cdot \mu + B \tag{5}$$

3. Circuit Implementation

3.1. Dynamic element matching

If the temperature error is limited to 0.1℃, the current ratio must be very precise. DEM seems a good choice to average out mismatches. Fig.2 shows how this method works. Two currents are in 1: 5 ratio, where one of the six current mirrors passes one transistor randomly and others passes the other. The current ratio has five possibilities. There will be errors between the possibilities and the ideal ratio. However, the mean of these errors is almost zero.

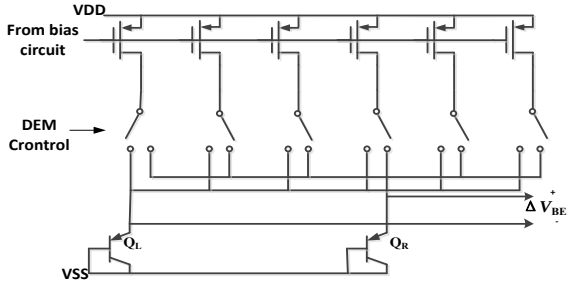

Fig. 2: Dynamic element matching circuit.

3.2. Bias Circuit

In CMOS process, the transistor can only be biased via its emitter, so the collector current *Ic* depends on the transistor's current gain β_{F}. A special circuit is taken to eliminate the effect of limited current gain [6]. Fig.3 shows the circuit diagram.

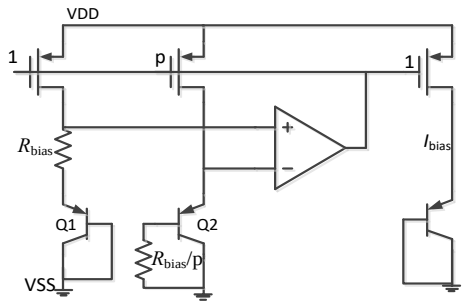

Fig.3: Elimination of current gain.

The two input voltages of operational amplifier are equal, so we can get:

$$V_{BE,Q1} + I_{bias}R_{bias} = mI_{bias}\frac{1}{1+\beta_F}\frac{R_{bias}}{m} + V_{BE,Q2} \tag{6}$$

The I_{bias} can be written as:

$$I_{bias} = \frac{1+\beta_F}{\beta_F}\frac{\Delta V_{BE,bias}}{R_{bias}} \tag{7}$$

And V_{BE} can be written as:

$$V_{BE} = \frac{kT}{q}ln\left(\frac{\beta_F}{1+\beta_F}\frac{I_{bias}}{I_S}\right) = \frac{kT}{q}ln\frac{kTln(p)}{qR_{bias}I_S} \tag{8}$$

From equation (8), the limited current gain has been eliminated.

3.3. Curvature Compensation

Fig.4 shows the error of result with different coefficient of V_{REF}.

If the V_{REF} has a positive temperature coefficient, then it can be written as:

$$V_{REF} = V_{REF0}(1 + xT) \tag{9}$$

where x is a very small temperature coefficient, and then:

$$\mu \propto \frac{1}{V_{REF}} \propto \frac{1}{1+xT} = 1 - xT + \frac{1}{2}(xT)^2 - \cdots \tag{10}$$

If we choose an appropriate temperature coefficient x, the nonlinearity of V_{REF} can be compensated by the first order term and the higher order terms can be ignored [7].

It can be seen that if the temperature coefficient of V_{REF} is 50ppm, the deviation from its nonlinearity is almost 0.1℃.

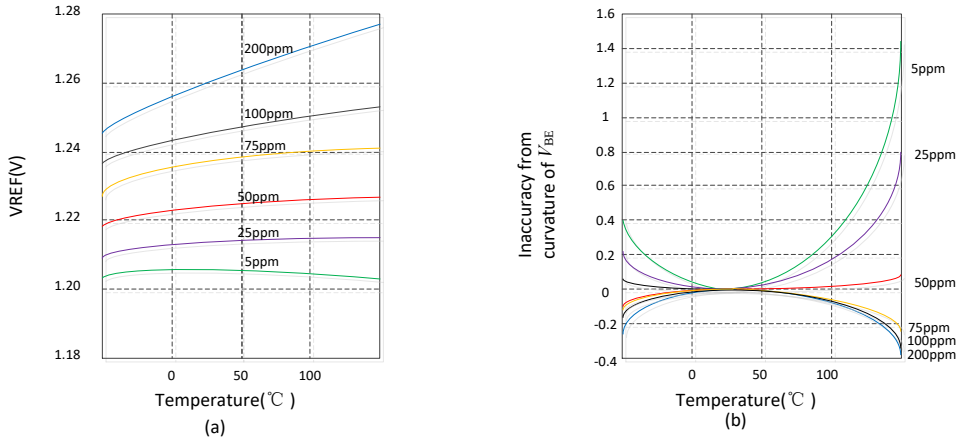

Fig. 4: (a) The reference voltage with different coefficient; (b) Deviation of the sensor.

3.4. SAR ADC

SAR ADC is chosen to quantify the PTAT voltage. To reduce the power consumption and area, split capacitor DAC is used. Fig.5 is the specific circuit.

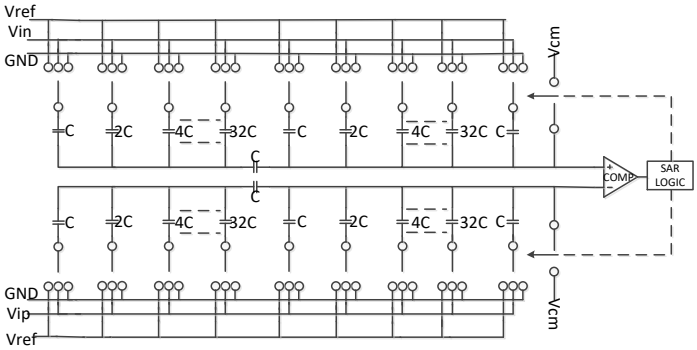

Fig. 5: The proposed SAR ADC architecture.

During the sampling phase, the bottom plates are connected with common voltage V_{cm}, the top plates of the most significant bit (MSB) capacitors while the compensation capacitor C_c are charged with V_{in} and V_{ip}. Then in the retention phase, all capacitors are connected to ground. Finally, the capacitor is connected to V_{REF} from the most significant to the least to accomplish successive comparison.

4. Layout and Simulation Result

The sensor is designed in TSMC 0.18μm CMOS process and simulated with the *Cadence Spectre*. The area of layout is 620μm×420μm. The layout is shown in Fig.6:

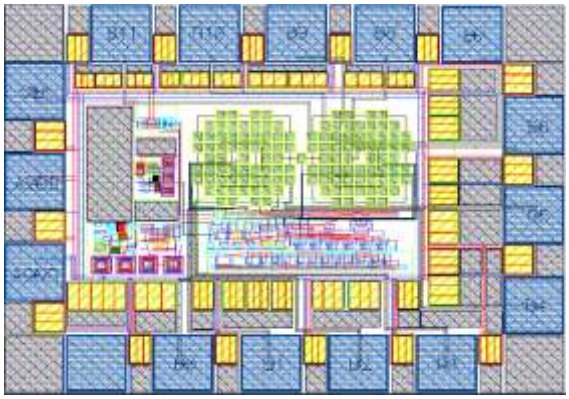

Fig. 6: Circuit layout.

Fig.7 shows the power spectral density of the SAR ADC. The sampling frequency is 10k Hz, where the SNR is 73.2dB and ENOB is 10.4 bit after simulation. Ten points are chosen to test the accuracy of the sensor. Two of them ensure the liner equation. Fig.8 shows the measured value and the real value of temperature. Fig.9 shows the deviation. The inaccuracy is below 0.5℃.

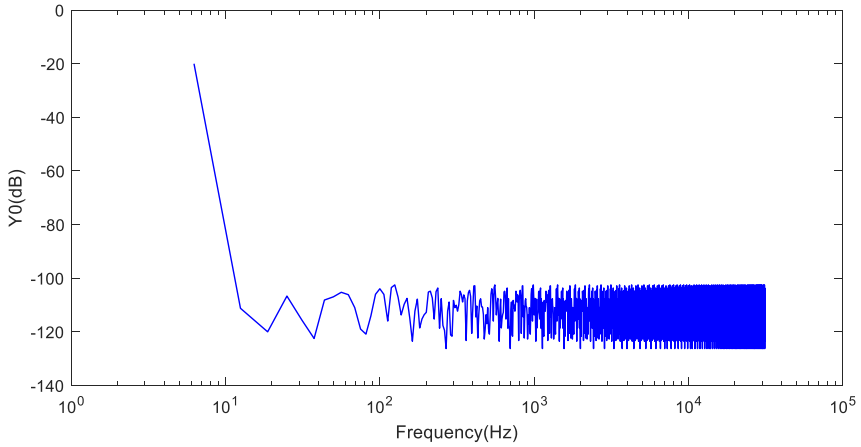

Fig. 7: Power spectral density.

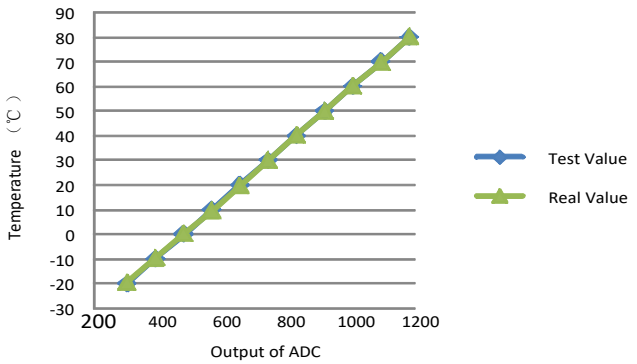

Fig. 8: Measured and real value of temperature.

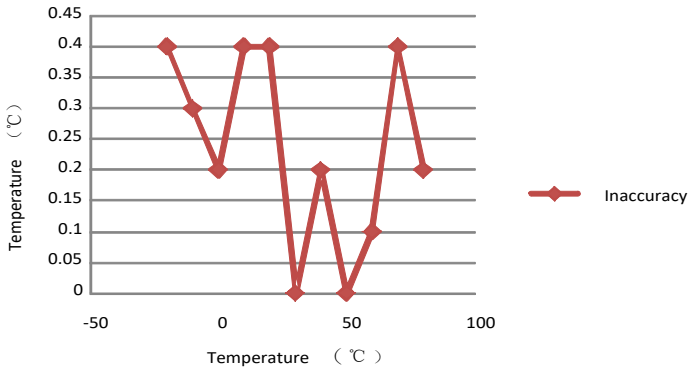

Fig. 9: Deviation between measured and real value.

The relationship between the output and the measured temperature is:

$$T = 0.1139 * D_{out} - 54.4 \tag{11}$$

Table 1: Performance Summary

Parameter	Simulation Result
Process	TSMC180nm
Supply Voltage	1.8V
Input Clock Frequency	100k Hz
Temperature Measurement Range	-20℃ to 80℃
Accuracy	0.5℃
Area	620μm×420μm
Power Consumption	1.25mW

5. Conclusion

The temperature sensor described in this paper achieves an inaccuracy of 0.5℃ over the temperature range of -20℃ to 80℃ in a 180-nm CMOS process. The main deviations are reduced by several techniques. An independent bias circuit is used to eliminate the current gain of the triode. Mismatch-related errors are eliminated with dynamic element matching. The nonlinearity of V_{REF} is compensated by a temperature-dependent reference. Meanwhile, a SAR ADC with split capacitor DAC is employed to reduce the power assumption and area.

6. Acknowledgement

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