ISBN 978-981-14-1684-2
Proceedings of 2019 the 9th International Workshop on Computer Science and Engineering
(WCSE 2019 SUMMER)
Hong Kong, 15-17 June, 2019, pp. 829-833
doi: 10.18178/wcse.2019.06.123

Design of Delay Cell and DLL Based on CMOS 65nm Process

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Abstract. With the development of analog integrated circuits, the characteristics of signal timing have a crucial impact on high-speed mixed-signal. Some delay cells can be designed to solve the delay differences and also they have been widely used in Delay Locked Loop (DLL), equalizer, and phased antenna arrays because it compensates the delay between the different signal paths. Moreover, the DLL's performance is largely determined by the delay unit. Therefore, the research and design of delay unit has important value and significance. The design and simulation are implemented by TSMC 65nm CMOS LP technology. DLL is made up of the Voltage Control Delay Line (VCDL), XOR gate phase detector and Voltage-Current (V/I) converter. The VCDL is implemented by cascading multi-level delay units, and the single delay unit uses active-inductor peaking technology to achieve wideband low-latency performance. The chip consumes a power of 31mW with 1.5V power and it occupies an area of 0.27mm^2 which including I/O pads. The delay time of designed single delay cell varies from 5.4ps to 7.1ps with 20% adjustment range within the bandwidth of 1-7GHz, showed from the post-layout simulation results. The design of the delay cell and DLL has some significance in the research of the low delay wide band delay circuit in the future.

Keywords: DLL, Voltage Control Delay Line (VCDL), TSMC 65nm CMOS LP.

1. Introduction

To achieve specific performance requirements, delay cells are needed usually in some circuit designing to offer compensations for the delay time between different signal paths. Time delay circuits are widely used in communication systems, FIR and IIR filters, the broadband beam-forming and equalizers e.g. [1, 2].

There are lots of methods to realize the time delay function, such as using transmission lines, lumped LC construction, or active devices. An excessive chip area is required in transmission line implementations [3]. Besides, the lumped LC delay line is also area-consumption as a result of the usage of inductances. What's more, there is a usually signal attenuation which restricts the number of cascading stages in the above two structures [4, 5]. In addition, both of them consume large power owing to the low impedance.

However, compared with delay line circuits mentioned above, the active delay line circuit has advantages in smaller area and power consumption [6,7].

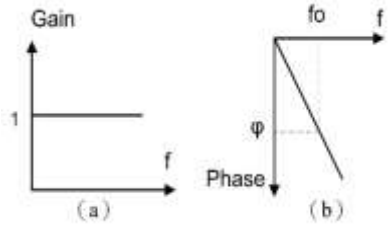

Fig. 1: Magnitude and phase

As we can see from Fig. 1, the gain-frequency characteristic and phase-frequency characteristic of an ideal delay line circuit are depicted in respectively. The ideal delay lines have a unity gain and its phase is

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also linear with frequency.

It is tougher to realise a constant true time delay because a delay circuit requires a constant ratio between $-\varphi$ and ω as well as a constant group delay which is independent of frequency. The characteristic of delay can be approximated well by exploiting the all-pass filter construction, e.g., a first-order all-pass filter:

$$h(t-\tau) \rightarrow e^{-s\tau} H(s) \tag{1}$$

$$H(s) = \frac{1 - s \cdot (\frac{\tau}{2})}{1 + s \cdot (\frac{\tau}{2})} \sim e^{-s\tau} \tag{2}$$

Both gm-RC filters and gm-C filters can realize the transfer function of the first-order all-pass filter. The delay cell need to provide accurate delay which is independent of external process, voltage, and temperature (PVT). A delay locked loop (DLL) is used to turn the delay properly. The DLL works with a reference frequency to stabilize the time delay. Besides the non-ideal factors of circuit also influence the locked delay.

This paper organized as follows. The fundamentals of a delay cell and DLL is introduced in the section 1. Section 2 presents circuit description. The circuit layout and the results of post-layout simulation is followed in Section 3 and draws the conclusions in Section 4.

2. Circuit Description

The DLL consists of delay cells, a multiplier, a V/I converter and a loop filter where is not just a single capacitor. The overall circuit architecture is depicted in Fig.2. Inputs of the amplifier AMP1 are composed of sinusoidal signal VIN and VIP which then pass through the voltage control delay line (VCDL) and the 相加 amplifier AMP2 to output node, VOUT. Both AMP1 and AMP2 is used for impedance matching. Due to the variations of process, voltage and temperature, the delay time of delay cells can change over large wide range. The DLL can provide compensation for these variations.

The description of loop working principle is as follows. The input sinusoidal reference signal, A•sin(ωt), is divided into two parts. The one accesses into the multiplier directly, the other one is passed into the voltage control delay line which is composed of M cascaded delay cell, then links to multiplier (M=9 in this paper). The delay of each cell is T_d s. After two signals which have different delay about M• T_d s is multiplied in the multiplier, there will be a DC error voltage whose expression is $1/2A^2\cos(M\bullet T_d)$ and a second harmonic component of $1/2A^2\cos(2\omega t+M\bullet T_d)$ which is filtered by the V/I module in multiplier's output node. The DC error voltage closed to 0 caused by the negative feedback means the input signals turn into orthogonal. As a result, the loop's total delay is T/4, while the delay cell delays (T/4)/M, where the T presents the cycle of reference signal.

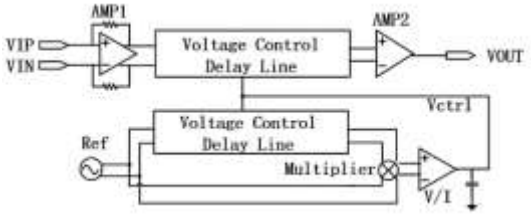

Fig. 2: DLL and the active delay lines out of loop

2.1. Active analog delay

Nowadays, there are many active delay line circuits. To get the group delay flatten over a broad band as well as have a wide 3dB bandwidth, a series of structures and technologies have been put forward. Specially, the active inductor shunt peaking and the source capacitive degeneration among them are more prominent.

Fig. 3 illustrates a kind of delay cell whose source uses the capacitive degeneration technology. The signal is input from the gate of differential pair M_1 and M_2 and output from its drain. The source of M_1 and M_2 connects to the R_5 so as to improve the circuit bandwidth. At the meantime, the circuit delay time can be adjusted through adjusting the C_S. The output resistance improves the linearity of the circuit and increases the output swing of the circuit as well. It is known that the circuit transfer function can be expressed as:

$$Av(s) = \frac{g_{m1} \cdot R_L}{(1 + g_{m1} \cdot \frac{R_s}{2})} \frac{1 + s\frac{R_s \cdot C_s}{2}}{(1 + sR_L \cdot C_L)(1 + s\frac{R_s \cdot C_s}{2 + g_{m1} \cdot R_s})} \tag{3}$$

From the transfer function, there are a LHP zero point z_1 and two pole points p_1 and p_2. When the operating frequency $\omega << z_1$, $\omega << p_1$, $\omega << p_2$, the group delay becomes a constant approximately:

$$\begin{aligned} GroupDelay(w) &= -\frac{\partial \varphi}{\partial \omega} \approx -\frac{1}{z_1} + \frac{1}{p_1} + \frac{1}{p_2} \\ &= R_L \cdot C_L - \frac{g_{m1} \cdot C_S \cdot R_S^2}{2g_{m1} \cdot R_S + 4} \end{aligned} \tag{4}$$

The source capacitive degeneration circuit changes the capacitor C_S by changing the D_{ctrl} to achieve the purpose of adjusting the delay.

The delay cell showed in Fig. 4 is used in this design. In this construction, the active inductor shunt peaking technology is carried out. As a zero point is introduced by the parasitic capacitors and resistances which are caused by between M_2's gate and source and the channel of M_3 respectively, the circuit bandwidth is extended. However, the small output swing caused by the heavy body effect of M_2 is the limitation of the active inductor shunt peaking technology. The gain of the delay cell at low frequency is given as follows:

$$Av = g_{m1} \cdot (Z_{in} // C_L) = \frac{g_{m1}}{sC_L + \frac{1}{R_{ds2}} + g_{mb2} + \frac{g_{m2} + sC_{gs2}}{1 + sC_{gs2}R_S}} \tag{5}$$

Where, Z_{in} is $(1+sC_{gs2}R_S)/ ((sC_L+1/R_{ds2})(1+sC_{gs2})+sC_{gs2}+g_{m2})$ and C_L is $C_{gd1}(1+A_V)+C_{db1}$.

The value of R_s (R_s is the turn-on resistance of M_3 in Fig. 4) can be adjusted by changing the size of V_{ctrl} and then the delay can be adjusted by transforming the zero point $1/(C_{gs2}R_S)$.

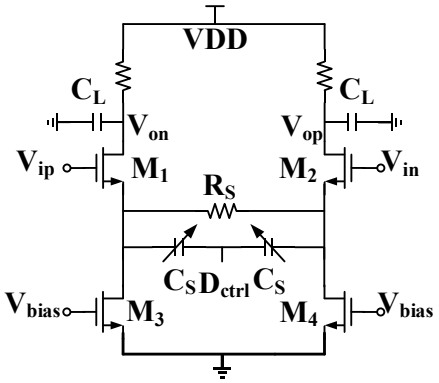

Fig. 3: Source capacitive degeneration

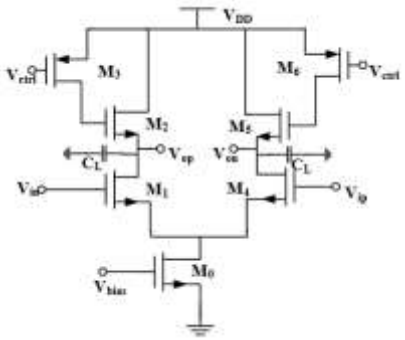

Fig. 4: Active inductor shunt peaking

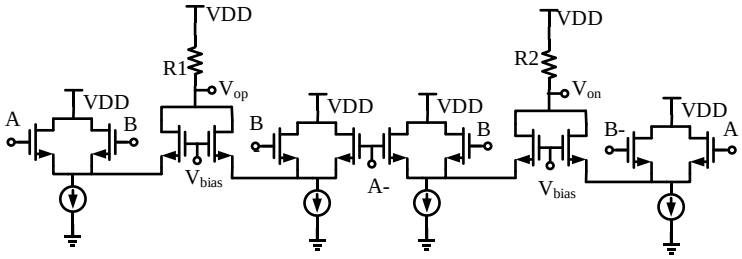

Fig. 5: Multiplier

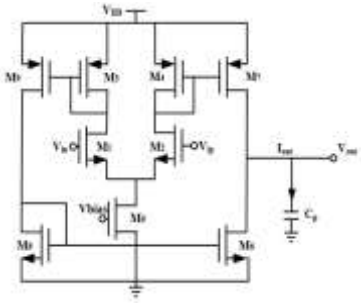

Fig. 6: V/I Converter

2.2. Multiplier

The multiplier showed in Fin. 5 is used in this design. Because of the asymmetry, there are some differences in propagation delay between two differential inputs in traditional multiplier. it must be insured that the multiplier is symmetry, or it will result some unwanted phase offsets. The multiplier works in a way as follows. If two inputs, A and B, are identical, there will be one of two tail currents flowing through R1, while no tail current flow through R2 on the right side. As a result, the output goes low. When the two inputs are not the same, the case reverses, too.

2.3. V/I Converter

A V/I converter is used to transform the voltage into current. Its construction is shown in Fig. 6. The accuracy of the loop delay is also affected by the offset and noise of V/I converter. So the layout of this module must be designed carefully.

3. Layout and Post Layout Simulation Results

The active delay lines and the delay locked loop (DLL) have been processed in TSMC 65nm CMOS LP technology. An area of 0.27mm^2 is occupied by the chip, the I/O pads included in.

As is shown in Fig. 7, there are a cluster of different group delay curves of the delay cell over the range of 1-7GHz when the control voltage changes from 0.1- 0.8V. The performance of delay cell vs the control voltage is showed in Fig. 8. It is shown that the bandwidth of circuit has a increasement and the group delay goes down with the control voltage increasing, because of the decreases of the variable capacitance.

Fig. 9 demonstrates that the loop delay is 57.3ps with a 4.4GHz reference frequency yet the ideal one is 56.8ps. Fig. 10 shows the characteristics of DLL output control voltage. Fig. 11 and Fig. 12 contrast the variation of loop delay time across temperature and process corners respectively between the delay line with DLL and the one without. It is shown that an added DLL helps the circuit to decrease delay variation caused by temperature changes and improve the sensitivity to process.

The layout of the designed delay locked loop and the active delay lines outside the loop is shown in Fig. 13.

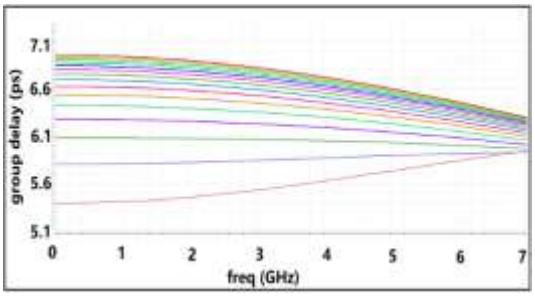

Fig. 7: Group delay for the unit active delay cell

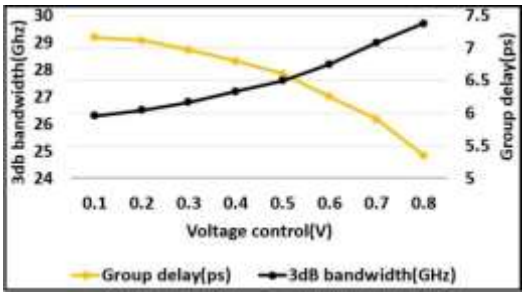

Fig. 8: Group delay and 3dB bandwidth for the unit active delay cell

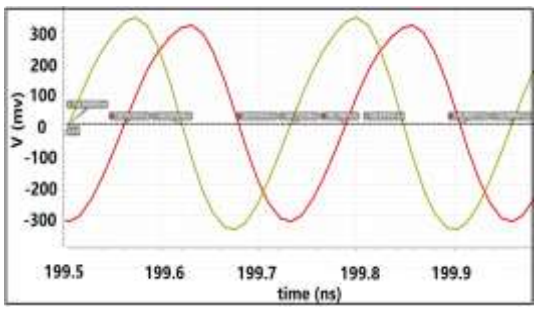

Fig. 9: Loop delay of DLL with reference frequency=4.4GHz

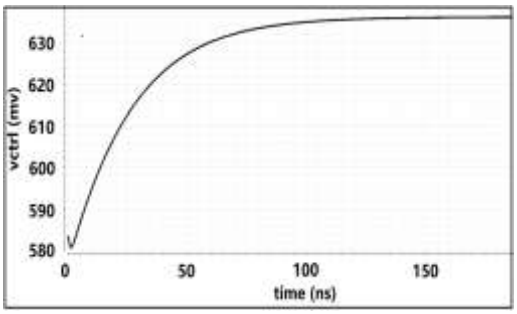

Fig. 10: DLL output control voltage

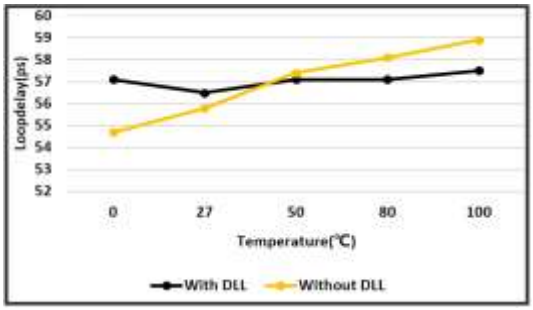

Fig.11: Loop delay variation across temperature

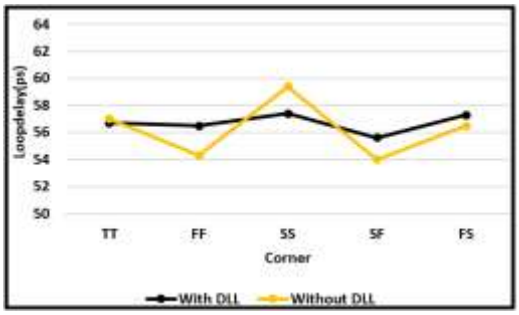

Fig. 12: Loop delay variation across process corners

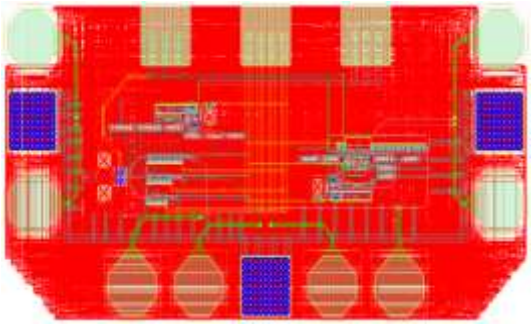

Fig.13: Layout of delay locked loop and the active delay lines out of loop

4. Conclusions

A compact all-pass delay cell whose delay time varies from 5.4ps to 7.1ps with a 20% adjustment rang is designed in this paper. There is a less than 3% delay variation over 1-7GHz. The delay cell has an at least 26GHz, even 30GHz 3dB bandwidth. In addition, a DLL circuit based on the delay cell is designed to maintain a good delay sensitivity over PVT. The whole chip which the I/O pads are included in occupies an area of 0.27mm^2 and consumes 31mW from a 1.5V supply.

5. Acknowledgements

This work is supported by Postgraduate Research & Practice Innovation Program of Jiangsu Province(SJCX18_0024), Natural Science Foundation of China (NO.61471119) and Academic Degree Postgraduate Innovation Project of Jiangsu Regular University (No. KYLX16 0215).

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