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Efficient Implementation of Adaptive Filter Architecture Using Gate Level Modification for ECG Denoising

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Abstract. A versatile channel assumes a critical part in clamor cancelation application. This paper introduces the gate level modified architectures for adaptive noise cancellation (ANC) using Matlab Simulink and Xilinx System generator and its implementation in XUP FPGA board. Gate level modification are done in Recursive Least square (RLS) filters to enhance the Signal to Noise ratio (SNR) and to optimize the VLSI parameters. The designed gate level modified structures are applied for noise cancellation in ECG Signals and Speech signals. The proposed gate level modified architectures shows better improvement in SNR, area and delay optimization respectively. From the results, it is clear that gate level modified RLS shows SNR improvement of 1.47% and 4.52% and shows area and combinational path reduction of 25.1% and 0.4% than basic RLS for 8-Tap filter respectively.

Keywords: adaptive filter, ECG denoising, RLS, SNR, Power Line Interference.

1. Introduction

The adaptive filter is termed as a filter which adjusts its transfer function by its own with respect to a particular algorithm. Generally in adaptive filter coefficients are updated at each cycle. There are many fields where adaptive filters are used such as identification of acoustic, estimation of channels, noise and echo cancellation techniques, biomedical signal processing, and adaptive control systems. In Adaptive filter transfer function is refined by using error control as feedback [1]. Signal to Noise Ration is the most common cost function that decides the performance of the adaptive filtering algorithms. A new approach of gate level modification in adaptive filters structure using different algorithms is proposed in this paper. Section 2 describes Adaptive Noise Cancellation technique and describes different adaptive filters algorithms such as RLS and Section 3 describes the proposed structure and how gate level modification is done in adaptive filter structures. Section 4 concentrates on the conventional adaptive filter structure for different adaptive algorithm. Section 5 describes the gate level modified adaptive filter structure using different adaptive filter algorithm.

2. Noise Cancellation in Adaptive Filter

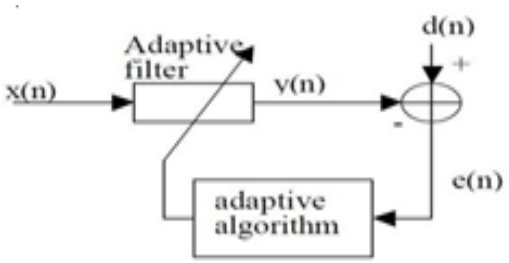

Fig. 1: Adaptive noise canceller block diagram.

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As shown in the Fig. 1, an Adaptive filter structure (ANC) has two inputs such as primary and subprimary input. The main role of primary input signal is to receive the signal from signal sources but the primary signal is naturally corrupted with noise.

RLS Algorithm

Recursive Least Square (RLS) algorithm is a widely used adaptive technique because of its fast convergence rate than other algorithms like LMS, NLMS [2]. At every iteration, the solution of new samples of the incoming signals is computed in recursive form [3]. RLS filter outperforms LMS filter by the factors such as fast convergence, utility of past available information in computation and no approximations in the algorithm.

Step 1: Weight Initialization $w(0) = 0$

Step 2: Inverse Correlation Matrix Initialization $P(0) = \delta\text{-}1IM$

Step 3: Compute Gain Vector $\pi(m+1) = P(m)u(m+1)$

$$k(m+1) = \pi(m+1)/\lambda + ut(m+1)\pi(m+1)$$

Step 4: Compute Error Estimate $e(m+1) = d(m+1)\text{-}wt(m)u(m+1)$

Step 5: Compute Inverse Correlation Matrix $P(m+1)=\lambda\text{-}1p(m)\text{-}\lambda\text{-}1k(m+1)ut(m+1)P(m)$

Step 6: Coefficients Updation $w(m+1)=w(m)+k(m+1)e(m+1)$ where λ is forgetting factor.

3. Gate Level Modification

Proposed architecture is the gate level modified implementation of adaptive filter. The gate level modification is implemented using modified EX-OR gate [4].The gate level modified half adder circuit is implemented using modified EX- OR gate is shown in Fig. 2. The total number of gates is reduced in the modified gate level representation of the EX-OR which implies in the reduction of Area and Delay [5] .

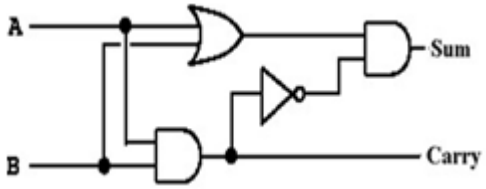

Fig. 2: Gate level modification for Half Adder circuit with modified EX-OR gate.

Sum = ((A|B)&(~(A&B))); Carry = A&B

This modified EX-OR gate is used for different Adaptive filter structure for designing gate level modified Architecture of RLS, AFFINE and KALMAN filters [4]. Initially gate level modification is done only in adder block of FIR part and gate level modification is done in adder block in both FIR part and Weight Updation part of the Adaptive filter. This gate level modified structure shows good result in SNR value, Area reduction and Combinational path reduction.

4. Conventional Adaptive Filters Design

4.1. ECG Signal Denoising

The outline is tried for commotion cancelation of ECG flag. ECG motion with the Power Line Interference (PLI) commotion is taken as the reference wanted flag for the reproduction [6], [7].The electrical cable obstruction (PLI) commotion which is 50 Hz sinusoidal wave is given as reference contribution to the channel [8]. At that point the denoised ECG flag is obtained by subtracting the channel yield from the coveted information. The input ECG signal is taken from MIT-BIH database (105.dat). The first 4000 samples are taken to the process and simulated in Matlab. Then this signal is used in Matlab Simulink by using signal from workspace block. The electrical cable obstruction (PLI) commotion which is 50 Hz sinusoidal wave, produced in Matlab and it is given as reference contribution to the channel utilizing signal from workspace square[9], [10].

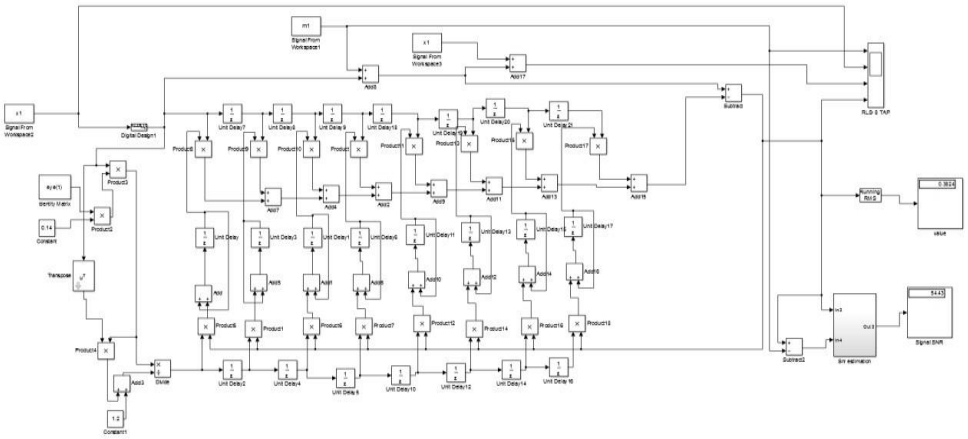

Fig. 3: Matlab simulink model for conventional 8-tap RLS filter.

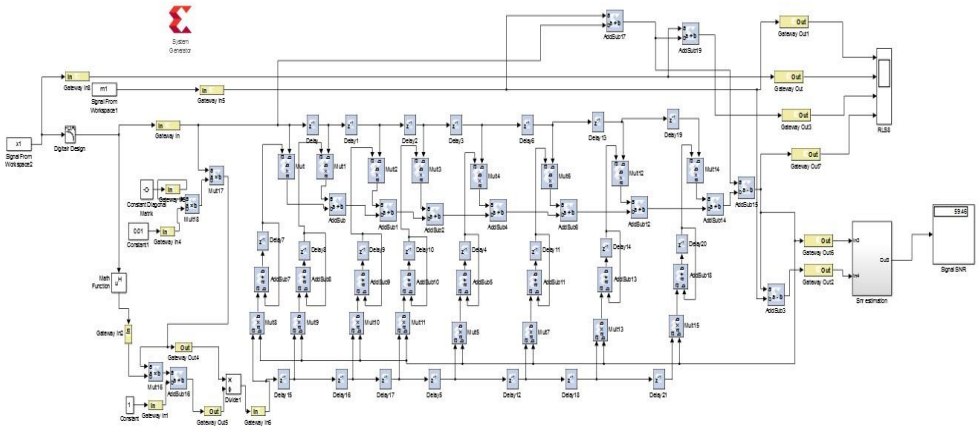

Fig. 4: Xilinx system generator model for conventional 8-tap RLS filter.

As shown in Fig. 3, the simulation of the Conventional 8- tap RLS filter for denoising ECG signal is carried out with the following parameters: Filter order N=8, forgetting factor λ=1 positive constant, δ=1,p= 4000. As shown in Fig. 4, the simulation of the conventional 8- tap RLS filter in sysgen for denoising ECG signal is carried out with the following parameters: Filter order N=8, step size μ= 0.2 and samples= 4000.

Fig. 5: Clamor cancelation output of ECG signal using conventional 8-tap RLS filter in Simulink

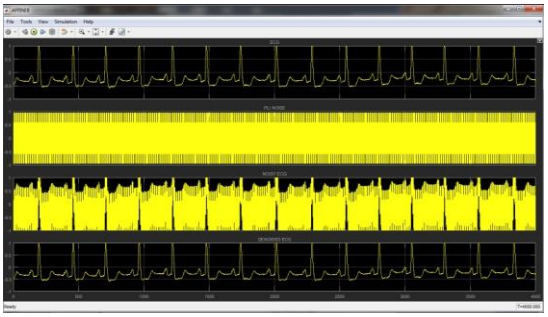

Fig. 6: Clamor cancelation output of ECG signal using conventional 8-tap RLS filter is sysgen.

In the Fig. 5 and Fig. 6, the main subplot demonstrates the information ECG signal (Rec.No.105), the second subplot demonstrates the PLI clamor, the third subplot demonstrates the debased ECG, the fourth subplot demonstrates the denoised ECG flag got utilizing traditional8-tap RLS versatile channels in Simulink and Sysgen.

4.2. Speech Signal Denoising

The designs are also tested for speech signal. Speech signal with the Gaussian noise is considered. The sampling frequency of the speech signal is 12000 Hertz. Gaussian noise of 0.1variance and zero mean is associated with speech signal. The original speech is corrupted with the Gaussian noise of specified specification. The output defines the clean speech signal with Gaussian noise effect with less percentage.

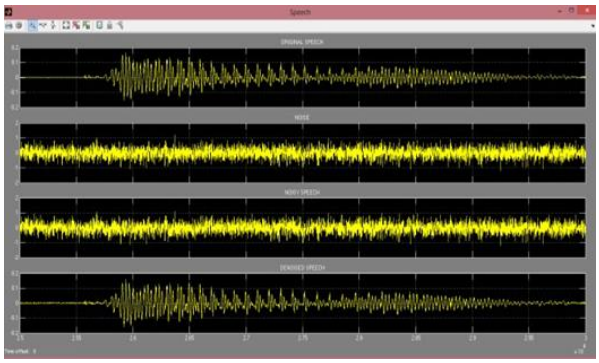

Fig. 7: Clamor cancelation output of Speech signal using conventional 8-tap RLS filter in Simulink.

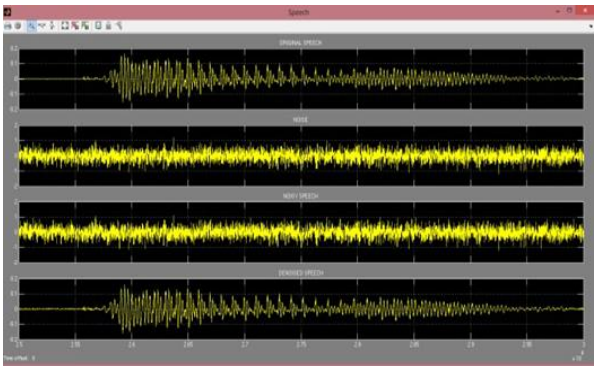

Fig. 8: .Clamor cancelation output of Speech signal using conventional 8-tap RLS filter in Sysgen.

The noisy speech is denoised by RLS adaptive filter perfectly and clear speech signal is obtained. The simulation for recovering the speech signal is carried out with the following parameters: N=8,λ=1, δ-1=1 and iterations= 32657 and Filter order N=8, μ= 0.2 and iterations= 32657 for proposed RLS filter. In the above Fig. 7 and Fig. 8, the first subplot demonstrates the information clean discourse flag, the second subplot demonstrates the Gaussian clamor, the third subplot demonstrates the defiled discourse flag, the fourth subplot demonstrates the recuperated discourse flag yield got utilizing traditional 8-tap RLS channel.

5. Adaptive Filters Design with Gate Level Modification

5.1. ECG Signal Denoising

The proposed designs 8-tap RLS filter structures with Gate level modification are designed in Matlab Simulink.

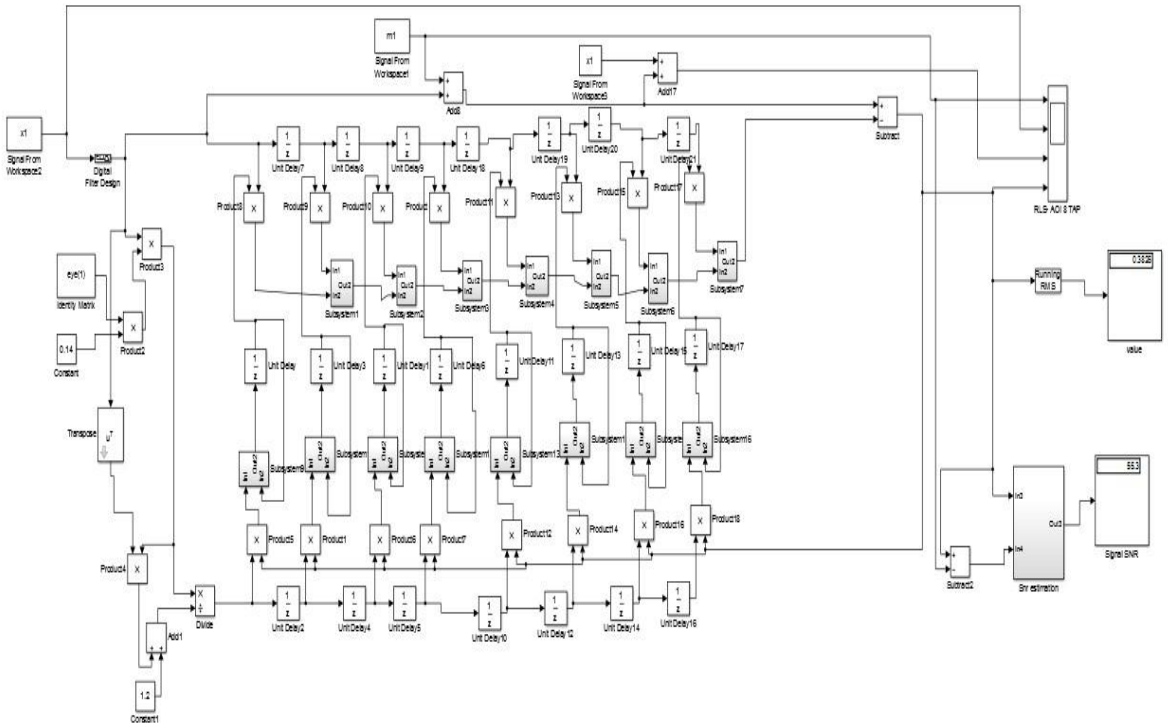

Fig. 9: Matlab simulink 8-tap RLS filter with gate level modification.

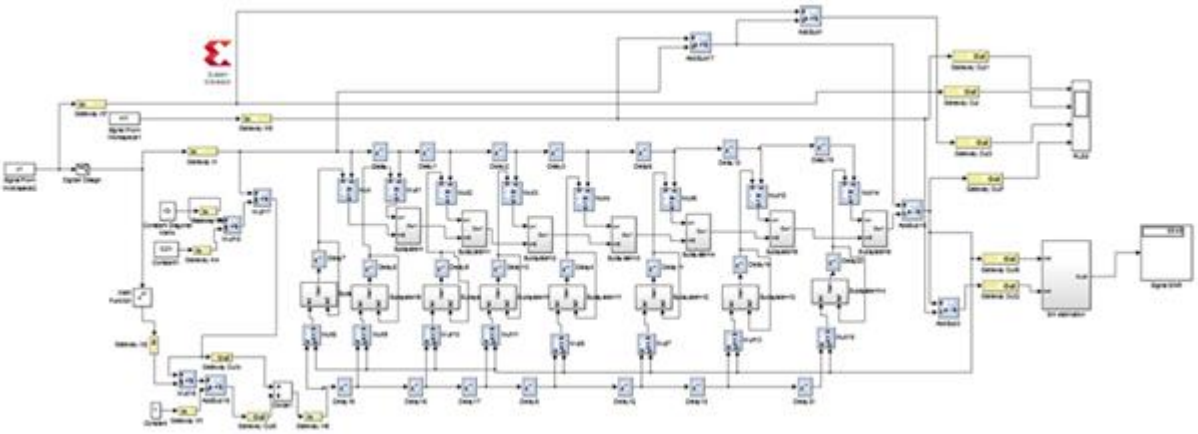

Fig. 10: Xilinx system generator model for 8-tap RLS filter with gate level modification.

Figure 9 and 10 shows the RLS structure with gate level modification in Simulink and Sysgen.

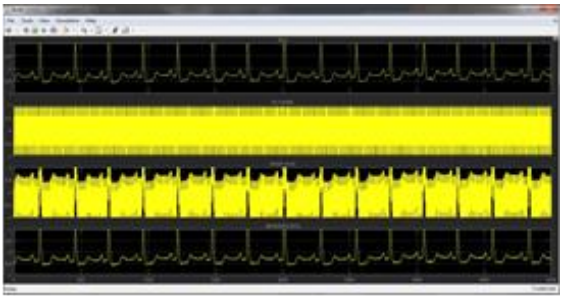

Fig. 11: Clamor cancelation output of ECG signal using modified 8-tap RLS filter in Simulink.

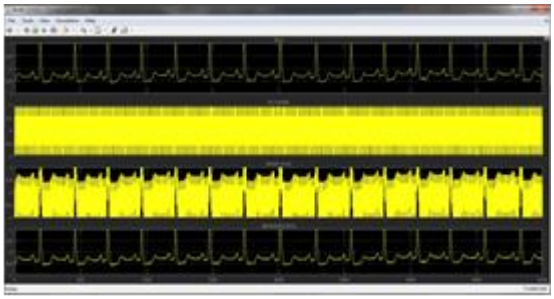

Fig. 12: Clamor Cancelation output of ECG signal using modified 8-tap RLS filter in Sysgen.

In the Fig. 11 and Fig. 12, the first subplot shows the input ECG signal (Rec.No.105), the fourth subplot shows the denoised ECG signal obtained using conventional and proposed RLS filter in Simulink and Sysgen.

5.2. Speech Signal Denoising

The designs are also tested for speech signal. Speech signal with the Gaussian noise is considered.

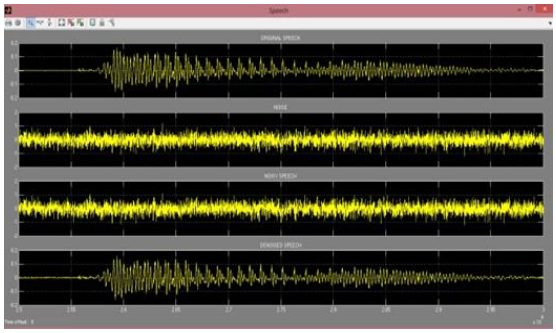

Fig. 13: Clamor cancelation output of Speech signal using modified 8-tap RLS filter in Simulink

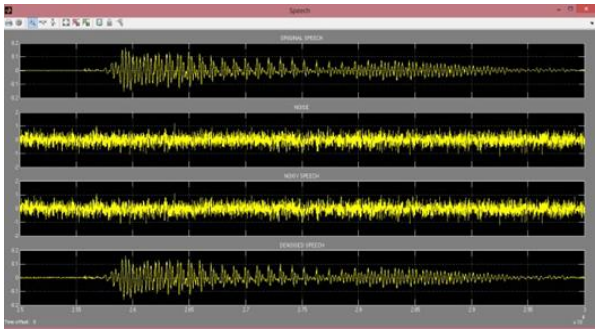

Fig. 14: Clamor cancelation output of speech signal using modified 8-tap RLS filter in Sysgen

Figure 13 and figure 14 represents the output of denoised speech signal with gate level modification in Simulink and Sysgen.

6. Performance Metrics for ECG and Speech Signal

The Performance metrics of the designed architecture is computed by estimating Signal to Noise ratio (SNR). SNR is evaluated using the formula.

$$SNR = 10\log_{10}\left(\frac{\sum_{k=0}^{M-1}(S_k)^2}{\sum_{k=0}^{M-1}(S_k - O_k)^2}\right)$$

Table 1: SNR estimation of 8-Tap RLS filter

INPUT ECG SIGNAL	RLS	MODIFIED RLS USING GATE LEVEL MODIFICATION
100.dat	53.62	54.3
101.dat	54	54.8
105.dat	54.43	55.3
108.dat	53.01	53.8
200.dat	57.43	58.2
203.dat	59.31	60.2
208.dat	60.34	61.18
228.dat	51.24	51.98
Average	55.42	56.24

Table 1 shows the estimated SNR value of 8-Tap RLS filter. Different Tap Lengths are used for the design and the performance is observed. The results obtained reveals that proposed RLS Adaptive filter structure with gate level modification in both FIR part and Weight Updation (WU) part shows an SNR improvement of 5.37%, 1.47% and 0.38% for 4-tap,8-tap and 16-tap RLS Adaptive filter structure respectively.

7. Implementation Results

Xilinx Virtex 5 FPGA is used for the implementation purpose. Hardware co-simulation is done after successful simulation. The bit stream file is automatically created in the co-simulation step and is associated with the JTAG Co- simulation block. The different parameters such as LUT, Number of Slices, Number of shift registers, Minimum period, Minimum input Arrival time before clock, Maximum output arrival required time after clock Combinational path delay is compared between Conventional and proposed architecture. The parameters such as LUT, Slice registers defines the architectural level of the adaptive filters confined the three basic VLSI parameters and the parameters defining the speed of the architecture is included to describe the clock speed and delay.

Table 2: Device utilization and timing summary for the conventional RLS and proposed RLS

Filter Length/ Parameter	4-TAP			8-TAP			16-TAP		
	RLS	MODIFIED RLS IN FIR PART	MODIFIED RLS IN FIR &WU	RLS	MODIFIED RLS IN FIR PART	MODIFIED RLS IN FIR &WU	RLS	MODIFIED RLS IN FIR PART	MODIFIED RLS IN FIR &WU
No. of Slice LUTs	642	592	528	1085	955	812	1947	1715	1367
No. of Slice registers	101	92	80	189	184	144	573	544	480
Min. period (ns)	26.16	21.734	19.944	33.97	21.89	20.1	48.73	22.273	20.505
Min. input Arrival time before clock(ns)	27.02	22.287	20.497	34.84	22.414	20.758	49.52	22.46	20.721
Max. output required time after clock(ns)	0.907	16.486	16.486	28.72	16.642	16.642	43.48	17.025	17.047
Max. Combinational path delay(ns)	33.35	33.35	33.35	33.35	33.35	33.216	44.27	32.467	32.071

Table 2 represents the resource utilization, combinational delay and various other characteristics for RLS algorithm. Different Tap Lengths are used for the design and the performance is observed. The results obtained reveals that proposed RLS Adaptive filter structure with gate level modification in both FIR part and Weight Updation (WU) part shows an Area reduction of 17.7%,25.1%and29.7%for4- tap,8-tapand16-tap RLS Adaptive filter structure and Combinational path delay reduction of 0.4%and 27% for8- tap and 16-tap RLS Adaptive filter structure respectively.

8. Conclusion

In this paper, the proposed entryway level adjusted design is connected to RLS versatile channel for compelling commotion cancelation in ECG flag and discourse flag. The results are taken in MATLAB and Xilinx System generator environment. The proposed gate level modified architectures shows better improvement in SNR respectively. The gate level modified RLS shows SNR improvement of 1.47% and 4.52% than basic RLS versatile channel structure for ECG flag and Speech flag and shows Area and Combinational way reduction of 25.1% and0.4%for 8- Tap filter respectively. The future work can be the implementation of gate level modification technique in different adaptive filters like Kalman and Affine adaptive filters.

9. References

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