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Narrowband Adjustable Time-Delay Line Design for Timed Array Antennas

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Abstract. A 4GHz–4.5GHz narrowband adjustable time-delay line circuit is presented for timed array antennas. The proposed architecture consists of a coarse tuning section and a fine tuning section. The coarse tuning is composed of delay cells and switch and digital control parts. A seven-stage delay cell with an active-inductor load design is used to provide a considerable range tuning capability with low normalised delay variation over a wide frequency span, and the insertion loss is approximately −29dB at 4.25GHz. The LC artificial transmission line in fine tuning section can provide continuous delay. The circuit is implemented in a 180 nm CMOS process and occupies a small area of 1.06 mm^2. The total relative delay can vary from 0ps to 200ps approximately, and the delay jitter is within 7%. The input return loss is better than -10dB, output return loss is better than -9dB. Under a supply voltage of 1.8V, the power consumption is only 46*1.8mW.

Keywords: Passive, active, delay line, CMOS.

1. Introduction

With the development of large-scale integrated circuits, time-delay lines have found applications in different areas, such as signal processing systems, telecommunications systems and phased array systems. In many of those applications it is required shaped beam patterns so that the antenna system can cover a wide coverage with similar level of power radiation, so timed array antennas are needed. It has been optimized for pencil and shaped beams by using isotropic sources with no mutual coupling. In the design of time-delay lines for integrated circuits, the size, insertion loss delay variation and bandwidth are major concerns. Various forms of active and passive delay elements have been used previously [1]- [3].

For digital applications, the delay in a stage can be realised by increasing the load capacitance in the switching stage, followed by an unloaded stage to restore the rise time of the digital waveform. This approach is not useful for implementing delays for analogue signals as they are sensitive to distortion. The concept of group delay is more important and relevant for analogue signals as opposed to the rise time or the propagation delay used in the digital domain.

In the analogue domain, the delay can be implemented by using passive discrete components, transmission lines or active circuits. Moreover, the delay cell should conserve area without excessive power consumption. This delay cell uses passive components in an active circuit and is used for delay-lock-loop (DLL) applications [4]. However, it is not acceptable in analogue circuits as it has tapped-delay lines made of cascaded delay stages. Therefore, we can use active and passive cells for a better result in analogue circuits [5].

In this paper, a new circuit architecture is presented in Section 2 and is described in detail in Section 3. The results and the layout are discussed in Section 4, and Section 5 presents the conclusion of this work.

2. Circuit Architecture

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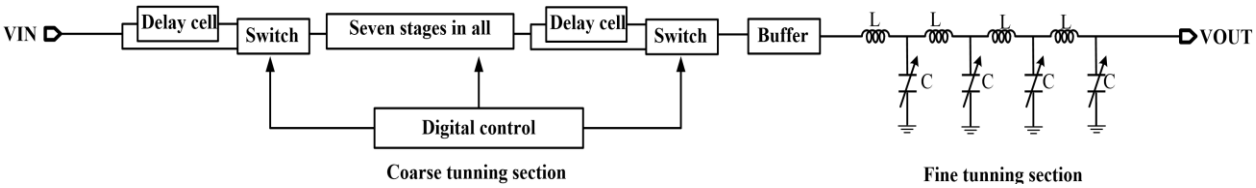

Fig. 1: Architecture of the proposed circuit.

Ideally, the delay cell should exhibit an exponential transfer function $H(s)=e^{-s\tau g}$, where τ_g represents the desired delay (or group delay). The circuit architecture shown in Fig. 1 has been proven to provide a reasonable group delay. It is organised by cascading the seven-stage shunt peaking active delay cells and the four-stage varactor-loaded LC artificial transmission line sections [7]. The delay of the unit shunt peaking active delay cell is τ_c, and the gain is 0dB. Active delay cells perform the function of coarse delay tuning along with the path selectors. The path selectors are achieved using switch1, switch2 and switch3. The continuous fine delay tuning is composed of L-networks with varactor-loaded LCs with the total τ_f ($\tau_f \geq \tau_c$), resulting in a continuous total delay. Moreover, the total delay is $\tau_f + 7*\tau_c$. The maximum variable delay can be extended by cascading more shunt peaking delay cells.

3. Building Block

3.1. Coarse Tuning Part

Figure 2 shows the equivalent model, which is a two-stage cascade common-source amplifier with a shunt inductance peaking load.

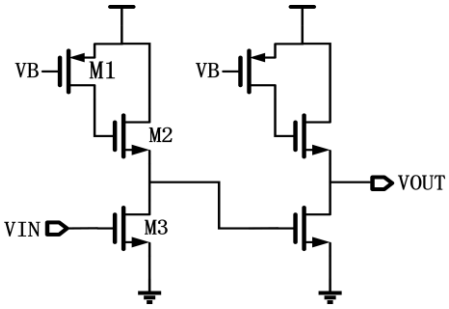

Fig. 2: Shunt inductance peaking active delay cell.

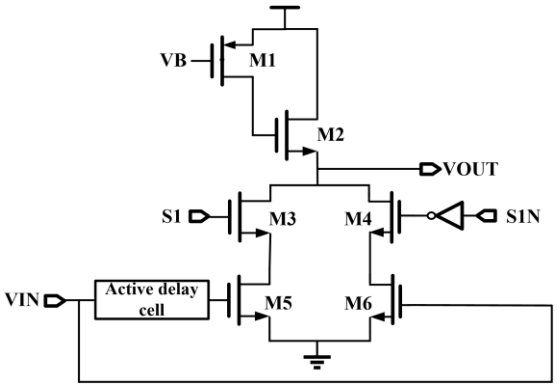

Fig. 3: Switch.

The gain of the unit amplifier can be expressed as follows:

$$A_V(\mathrm{s}) = \frac{g_{m1}(1+sC_{gs2}R_g)}{g_{m2}+s(C_{gs2}+C_L)+s^2R_g(C_{gs2}+C_L)} \tag{1}$$

where C_L is the load of the capacitances. Further, the two poles are at

$$-\frac{1}{2}\cdot\left(\frac{C_L+C_{gs2}}{C_L\cdot C_{gs2}\cdot R_g}\right)\pm\frac{1}{2}\cdot\sqrt{\left(\frac{1}{C_L\cdot R_g}+\frac{1}{C_{gs2}\cdot R_g}\right)^2-\frac{4g_{m2}}{C_L\cdot C_{gs2}\cdot R_g}} \tag{2}$$

The zero is at $1/R_gC_{gs2}$. By varying R_g (R_g is the turn-on resistance of M1 in Fig. 2), we can control the zero location. The relationship between poles, zeros and the group delay can be expressed as follows:

$$GD(\omega) = -\frac{1}{1+(\omega/Z_1)^2}\cdot\frac{1}{Z_1}+\frac{1}{1+(\omega/P_1)^2}\cdot\frac{1}{P_1}+\frac{1}{1+(\omega/P_2)^2}\cdot\frac{1}{P_2} \tag{3}$$

Thus, the group delay of the coarse delay cell can be flattened by assigning a suitable value of zero. Voltage gain is another element that should be noted. By using a switch, we obtain two signal paths. Therefore, 0dB voltage gain is necessary.

In Fig. 3, the design of the analogue switch is illustrated. It acts as a path selector to achieve coarse tuning. S1 and S1N are the digital voltages that are provided by the digital control cell to select the signal paths. If S1 is low, S1N is high and vice versa. Note that M5 and M6 are of the same size, and M3 and M4 are the same.

To enhance the −3dB bandwidth of the delay line, the shunt inductance peaking load is also used in the analogue switch.

3.2. Fine Tuning Part

Fig. 4 shows the design of the four-stage LC fine tuning part.

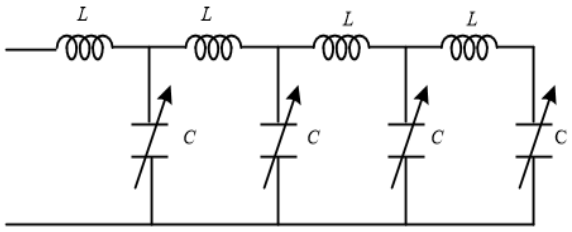

Fig. 4: Cascaded LC delay cell.

The characteristic impedance of the unit LC L-network can be expressed as follows:

$$Z_0 = \sqrt{L/C} \tag{4}$$

Further, the group delay can be expressed as follows:

$$\tau = \sqrt{LC} \tag{5}$$

The cut-off frequency of the unit LC L-network can be expressed as follows:

$$\omega = 1/\sqrt{LC} \tag{6}$$

The selection of suitable values of the varactors and the inductors is critical in LC delay cells.

3.3. Buffer

To obtain the same load as that in the previous stages and enhance the −3dB bandwidth of the buffer, an active delay cell is required [8]. The output impedance of the source follower is approximately $1/g_{m4}$, it can be used to match the LC L-network. The buffer circuit is shown in Fig. 5.

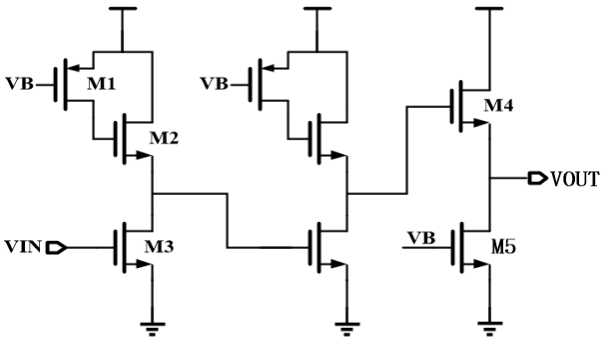

Fig. 5: Buffer architecture.

4. Layout and Simulation Results

A fully integrated delay line has been implemented using the 0.18μm CMOS technology. The core of the delay line with I/O pads occupies an area of less than 1.06mm². Fig. 6 shows the layout of the proposed circuit. The insertion loss of the proposed circuit is approximately −29dB at 4.25GHz. Figs. 7 and 8 show the simulated absolute delay and the relative delay of the seven states, respectively. Fig. 9 shows the simulated time-domain delay response. Note that the time-domain delay response has some differences from the group delay.

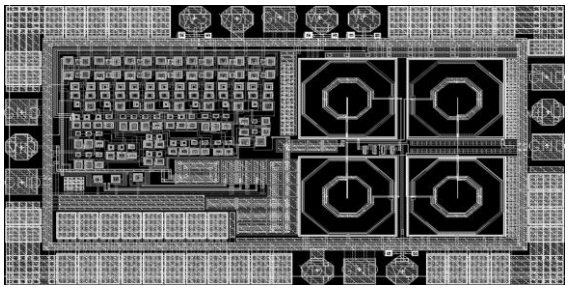

Fig. 6: Layout of the circuit.

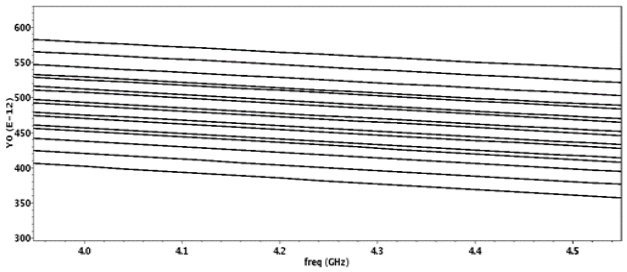

Fig. 7: Absolute delay of the circuit.

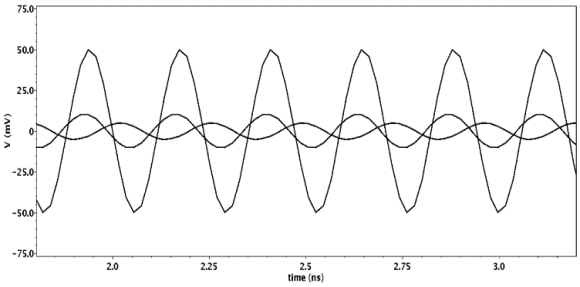

Fig. 8: Relative delay of the circuit.

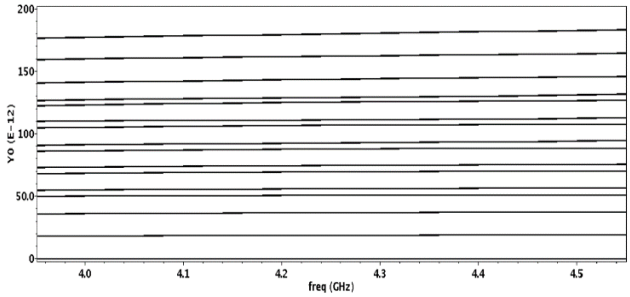

Fig. 9: Time-domain delay response@4.25GHz.

The simulated result is listed in Table I and compared with other recently reported delay line circuits.

Table 1: Performances summary

Reference	This work	[6]	[7]
Supply Voltage(V)	1.8	2.5	2.5
DC power(mW)	82.8	87.5	268.5
Frequency(GHz)	4.5-5	0-13	22-37
Max delay(ps)	200	64	17.8
Chip size(mm^2)	1.06	2.25	0.31
Technology	0.18 μm CMOS	0.18 μm BiCMOS SiGe	0.25 μm BiCMOS SiGe

5. Conclusion

A narrowband adjustable time-delay line design for integrated circuits with a wide continuous range is proposed in this paper. With coarse delay tuning and fine delay tuning, we achieved a flat delay response from 4GHz to 4.5GHz. The future work is to be able to maintain flat gain and group delay over an ultra-wide bandwidth.

6. Acknowledgments

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