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Low-Power High-Speed 8-Bit Shift Register Using Double-Edge Triggered Flip-Flops

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Abstract. This investigation presents an 8-bit shift register based on a lower-power double-edge triggered (DETFF) flip-flop. The 8-bit shift register based on the low-power DETFF is carried out by using Cadence Virtuoso version 5.1 and TSMC 0.18 μm CMOS technology. The major contribution of the proposed design is a method using a double-clocking technique to latch data bits such that shorter time delay and the less power dissipation are achieved at the same time. The all-PVT-corner (process, voltage, temperature) post-layout simulation results demonstrates 34.970 mW at the highest 125 MHz clock rate.

Keywords: shift register, DETFF, low power, post-layout simulation, all-PVT.

1. Introduction

The demand of portable consumer electronics powered by batteries is fast growing in the market. IC designers are facing the challenge of keeping low-power consumption thereof to extend the operation time. Each module of a digital system required appropriate design for the lowest possible power to keep the pace with the scaling of technology, e.g., a single chip integrated by billions of transistors using nano-scale CMOS processes [1] [2].

In VLSI technology, digital circuits obtained the edges of the speed, area and power, where the flip-flops and latches are the key sub-circuits. They often consume large space for VLSI implementation on silicon. Certainly, they are highly correlated to speed, power, and accuracy. Notably, the output of combinational logic circuit depends on the present input. By contrast, that of the sequential logic circuit depends on both present input and previous output or present state such that flip-flops or the registers (memory) are needed. Every operation in digital circuit, e.g., shift, addition and multiplication, is carried out through registers and the associated data movement therewith [3].

Generally, the memory (register) is able to load data and output data. Flip-flops can be assembled to consist of registers to execute a function for shifting the data. In other words, a shift register is a type of logic circuits that was used essentially in the storage of digital data. Moreover, a universal shift register is well known to perform not only parallel and serial shift, but also load data in parallel or in serial. For example, Serial In Serial Out (SISO), Serial In Parallel Out (SIPO), Parallel In Parallel Out (PIPO), and Parallel In Serial Out (PISO) all can be carried out by the universal shift register [3] [4].

DETFF (Double-Edge Triggered Flip-flops) [5] was reported to take advantage of a clocking technique or fasten the digital throughput, which consumes less power without sacrificing data rate. That is, the frequency of the clock will be reduced by half if DETFF is used to keep the same throughput. Referring to Figure 1, a classic double-edge triggered flip-flop is shown, where two opposite polarity level-sensitive latches, D1 and D2, are positive level-sensitive and negative level-sensitive latches, respectively, are used. M1 is a multiplexer governed by the equation: $y = d_0\,\bar{s} + d_1\,s$. When the clock signal is high, the latch D1

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is transparent and M1 selects the value stored in the latch D2 coupled to output Q. By contrast, when clock turns low, the latch D2 becomes transparent, and the data bit stored in Dl is multiplexed to the flip-flop output Q. Therefore, the stored data can be output at either rising edge or falling edge of the clock such that it is a DETFF [6]. However, this design results in high power dissipation and large area, since too many logic gates are needed.

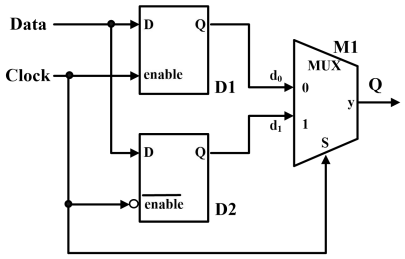

Fig. 1: Typical DETFF implementation.

Therefore, a novel DETFF taking advantage of transistors with different Vth is used to consist of an 8-bit shift register so as to resolve all of the mentioned issues. The design is realized using TSMC 0.18μm CMOS technology. Detailed all-PVT-corner (process, voltage, temperature) simulations are carried out to justify the impressive performance.

2. 8-Bit Shift Register Design

2.1. DETFF using transistors with different Vth

A novel flip-flop proposed by Wang *et al.* [7] is 1-bit double-edge triggered flip-flop as shown in Figure 2. The transistors A1 to A4 consisting of an XOR gate, which is like an edge detector generator to detect the edge transitions as well as the inverter chain, InvA to InvD, have nothing to do with the state transition at Vinput and stage1. Therefore, it is no need to pay the price of large area and high leakage current by employing low-Vth to carry out the XOR gate and the inverter chain.

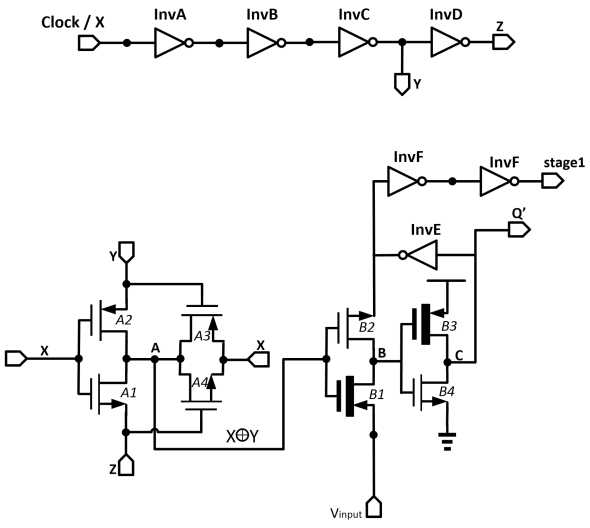

Fig. 2: Previous DETFF designed by Wang [7].

Referring to Figure 2, Vinput is coupled to the source of PMOS B1 such that the state of node B is expected to follow Vinput. Apparently, it is a common-gate amplifier formation of which gain is proportional to its gm_{B1}, the transconductance of B1, where $gm_{B1} \cong (V_{GS} - V_{th})$. Therefore, a low-Vth transistor is a better selection to achieve high speed and low power at the expense of a large area. B3 and B4 consist of an inverter to drive InvE. Meanwhile, the input of this inverter, i.e., node B, is the output of another inverter composed of B2 and B1. The inverter composed of B2 and B1 is a "floating" inverter where

there is no path to VDD or GND. Therefore, node B becomes a “weak” output to drive the inverter of B3 and B4, where B3 is the current source and B4 is the current sink. This then becomes an issue to be resolved. If B3 is a high-Vth transistor, it will suffer from the problem of having to supply a large current to drive InvE in addition to the fact that the “weak” node B cannot easily switch it on. Hence, B3 should be a low-Vth transistor.

2.2. Timing of the inverter chain

Figure 3 shows the waveforms generated by the inverter chain in Figure 2. The system clock signal CLK also (labeled X) is inverted and delayed a certain amount of time to generated the signal, labeled Y, via 3 cascaded inverters. An XOR operation of X and Y will generate a periodical signal whose frequency was double of that of the clock signal, X, with a non-50% duty cycle. The reason why the duty cycle of the periodical signal, X ⊕ Y, is less than 50% is that only a short period of logic low (0 level) is needed to carry out the following latch operation [7][8]. The short period condition is when the signal awareness of the XOR all-PVT-corner output nudges the momentary X axis, or at the 0 level.

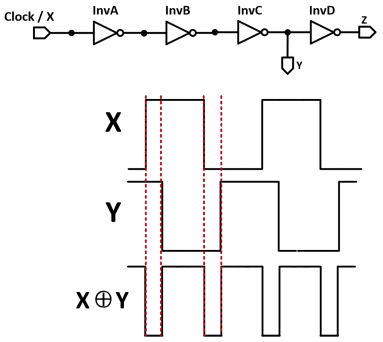

Fig. 3: Generation of X Y.

2.3. 8-bit shift register using DETFFs

The entire shifter circuit in Figure 4 is elaborated in Figure 5 to demonstrate how those 8 stages are assembled. Figure 5 is block diagram of the proposed 8-bit Shift Register, including three blocks. Firstly, Clock Generator is in charge of generating timing signals. Secondly, XOR Array collects edges from the outputs of Clock Generator, and the last, Low-power Latches acquire all of the data bits.

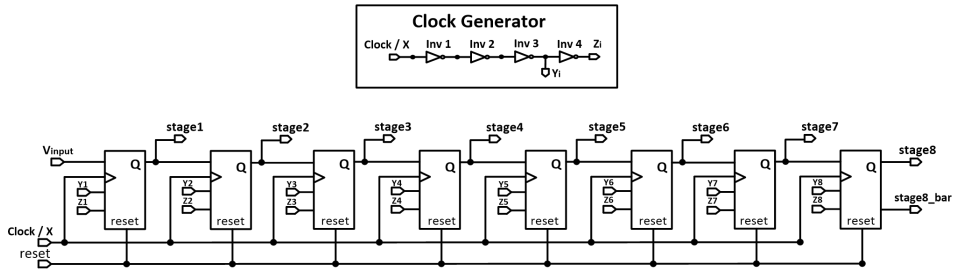

Fig. 4: Schematic of the 8-bit shift register.

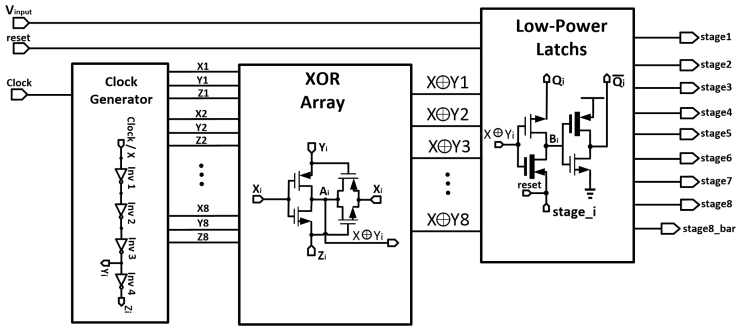

Fig. 5: 8-bit shifter register circuit block diagram.

3. Implementation and Simulation

3.1. Pre-layout simulation

The proposed design is implemented using TSMC typical 0.18 µm CMOS technology. Figure 6 demonstrates the pre-layout simulation result, which shows that the data pulse are moved forward from stage1 to stage8 as expected. To verify the reliability of the proposed design, we then ran all-PVT-corner simulation before layout, as shown in Figure 6. Not only is the functionality verified correctly, but the highest speed is also found to be 125 MHz. Notably, process corners are TT, SS, FF, FS, and SF. Supply voltage variation cover three supply voltages, 1.62 V, 1.8 V and 1.98 V. The temperature corners are 0°, 25°, 50°, 75° and 100° C.

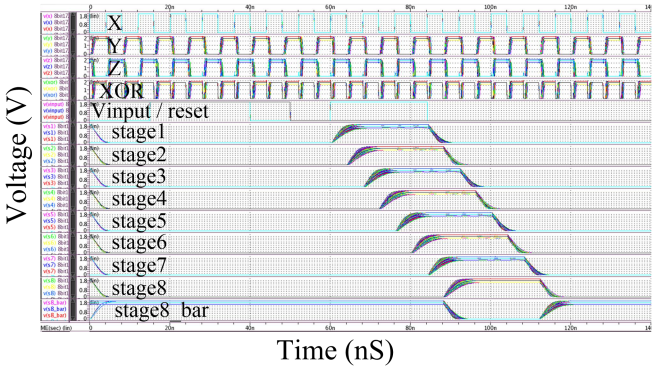

Fig. 6: Pre-layout simulation result.

3.2. Layout design and post-layout simulation

Figure 7 shows the whole chip layout of the 8-bit shift register using double-edge triggered flip-flops with guard rings. The chip area is 888×628 µm^2. The whole chip layout was developed in Virtuoso Layout Editor, and post-layout simulation was carried out using HSPICE. A total of 174 transistors are used, where the power dissipation is 3.497 x10^{-2} W at the maximum frequency of 125 MHz obtained from HSPICE simulation. Figure 8 shows post-layout all-PVT-corner simulation result.

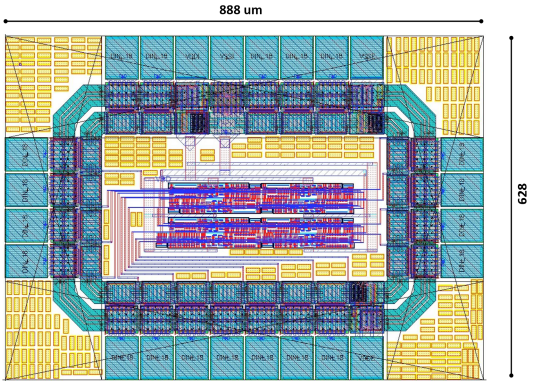

Fig. 7: Chip layout of the proposed 8-bit shift register.

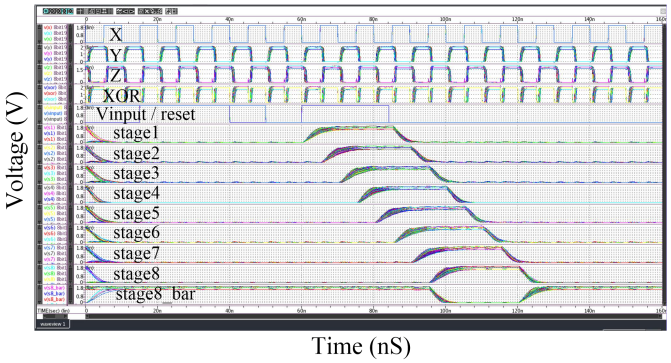

Fig. 8: All-PVT-corner simulation result (post-layout).

3.3. Performance comparison

Table 1 tabulates the proposed double-edge triggered performance comparison with those of several prior works. To compare the performance of different designs, an FOM (Figure of Merit) is needed, which is defined in the following equation. Referring to the FOM in Table 1 with all of the same frequency are 125 MHz, our design attains the second best FOM of all the listed designs. Notably, the requirement of measurement is to drive 20 pF because of the need to drive large loads.

$$FOM(Figure\ of\ Merit) = \frac{Power \times Delay}{bits \times freq \times C_{load}}$$

TABLE I: COMPARISON WITH PRIOR WORK

Case	Circuit	Year	Power Supply	Rise delay (ps)	Fall delay (ps)	Pwr (μW)	P · D (fJ)	Number of bit	Load (pF)	CLC (MHz)	FOM
1	[8]	2004	1.5 V	410	402	47.8	19.6	1	0.1	125	$1.56x10^{-9}$
2	[7]	2006	1.5 V	503	765	66.3	50.5	1	0.1	125	$4.05x10^{-9}$
3	this work										
	Pre-layout	2017	1.8 V	1660	1460	32390	187590	8	20	125	$2.68x10^{-9}$
	Post-layout	2017	1.8 V	2220	2210	35220	7820	8	20	125	$3.90x10^{-9}$

4. Conclusion

In this investigation, an 8-bit shift register is designed based on double-edge triggered flip-flops (DETFF). It is realized by TSMC typical 0.18μm CMOS technology. The feature of the design is that transistors with different Vth are used in the DETFF, where 2 of the devices are analysed and replaced with low-Vth transistors to achieve a low-power and high-speed shifter design.

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