ISBN 978-981-11-3671-9
Proceedings of 2017 the 7th International Workshop on Computer Science and Engineering (WCSE 2017)
Beijing, *25-27 June*, *2017*, *pp. 1099-1102*
doi: 10.18178/wcse.2017.06.191

A Low Power Quadrature Voltage Controlled Oscillator Design for 2.4GHz ISM Band Application

Tung Hsu Wu [1], Zong Ru Wan [2+] , Bo Jia Chan [3] and Chang Hsi Wu [4]

[1, 2, 3, 4] Lunghwa University of Science and Technology, LHU, Taoyuan, Taiwan

Abstract. A low power Quadrature voltage controlled oscillator (QVCO) design for 2.4GHz ISM band, fabricated by using CMOS 0.18um process, is presented in this paper. The tuning range of the proposed QVCO is mainly broadened by a novel negative resistance, variable capacitance and tapping inductance design. Simulation results of the proposed QVCO reveal phase noise of -111@1MHz and tuning range of 2.02GHz~2.549GHz (23.1%) while consumption is 4.93mW under the supply voltage (V_{dd}) of 1.2V and control voltage (V_{ctrl}) of 0.7~1.8V. The core area of the designed chip is 1.2mm*1.2mm.

Keywords: QVCO, 0.18um, negative resistance, variable capacitance, tapping inductance, CMOS.

1. Introduction

In recent years, most of the RF transceivers used four-quadrant IQ architecture due to high transmission rate and reliability. In order to apply this circuit architecture, many scholars put forward the key QVCO design. In 2002, Sabine Hackl, Josef Bock and Guntor Ritzberger proposed the SiGe Bipolar process to implement QVCO, but it made the phase noise poor [1]. Therefore, the technology of CMOS LC tank was proposed to improve the phase noise by Pietro Andreani, Andrea Bonfanti, Luca Romano and Carlo Samori, but the power consumption was 50mW [2]. In order to improve the power consumption problem, Hye-Ryoung Kim and Seung-Min Oh used the Back Gate Coupling technology to achieve low power consumption. The power consumption was 5.4mW [3].

To achieve sufficient frequency tuning range, the proposed circuit in this paper not only allows a coarse-tuning voltage (V_{ctrl}) to vary from 0.7V~1.8V, but also has a fine-tuning bias (V_b) to increase the compensability of the circuit. In addition, the power consumption of this chip is only 4.9mW. To avoid any mismatch problems when connecting the chip to the other circuit or instrument, buffers used as matching circuits are designed at all 4 outputs.

2. Circuit Design

The QVCO circuit proposed in this paper is shown in Fig. 1. Using V_b to do tail current control can not only effectively control power consumption; it can also create an equivalent negative resistance through the coupling capacitor. This connects to the novel negative resistance formed by Q_1, Q_2, Q_3 and Q_4 in the circuit to achieve low power consumption to counteract the loss of the resonant LC tank.

In the equivalent half-circuit in Fig. 2, the capacitance C contains the variable capacitance and the parasitic capacitances of the transistors, G is the equivalent transconductance representing the inductance loss.

[+] Corresponding author. Tel.: + 886 922 348 418
E-mail address: computerisgood@gmail.com

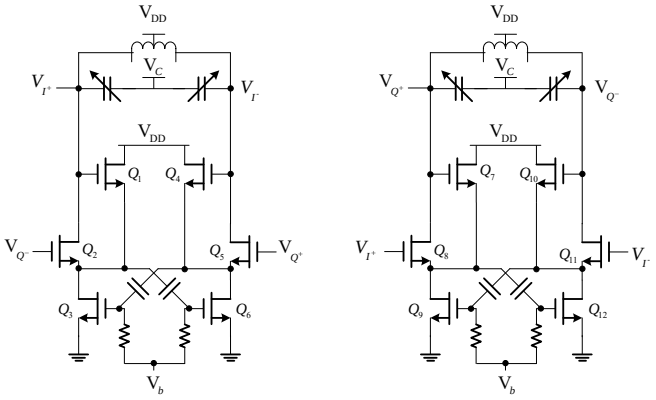

Fig. 1: Circuit architecture diagram

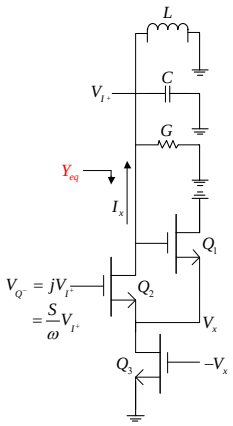

Fig. 2: Circuit analysis diagram

From Fig. 2, it can be seen that

$$V_x = \frac{g_{m1}V_{I^+} + jg_{m2}V_{I^+} + g_{m3}V_x}{g_{m1} + g_{m2}}$$

Then

$$I_x = g_{m2}(V_X - jV_{I^+}) = g_{m2}\frac{g_{m1} + j(g_{m3} - g_{m1})}{g_{m1} + g_{m2} - g_{m3}}V_{I^+} \tag{1}$$

In addition, during oscillation

$$\frac{1}{G + j(\omega_0 \mathrm{C} - \frac{1}{\omega_0 L})} I_x = V_{I^+}$$

Substituting into (1), we obtained

$$G + j(\omega_0 \mathrm{C} - \frac{1}{\omega_0 L}) = g_{m2}\frac{g_{m1} + j(g_{m3} - g_{m1})}{g_{m1} + g_{m2} - g_{m3}} \tag{2}$$

Then the oscillation condition and oscillation frequency can be written as

$$G = \frac{g_{m1}g_{m2}}{g_{m1} + g_{m2} - g_{m3}} \tag{3}$$

$$\omega_0 C - \frac{1}{\omega_0 L} = g_{m2}\frac{g_{m3} - g_{m1}}{g_{m1} + g_{m2} - g_{m3}} \tag{4}$$

, respectively. In addition, the admittance formed by the active element during oscillation is

$$Y_{eq} = \frac{-I_x}{V_{I^+}} = -g_{m2}\frac{g_{m1} + j(\mathrm{g_{m3}} - \mathrm{g_{m1}})}{g_{m1} + g_{m2} - g_{m3}} = G_{eq} + jB_{eq} \tag{5}$$

where the equivalent negative conductance and susceptance are

$$G_{eq} = -\frac{g_{m1}g_{m2}}{g_{m1} + g_{m2} - g_{m3}} \tag{6}$$

$$B_{eq} = \frac{g_{m2}(g_{m1} - g_{m3})}{g_{m1} + g_{m2} - g_{m3}} = \frac{1}{\omega_0 \mathrm{L}} - \omega_0 C \tag{7}$$

, respectively. In the design, to reduce the oscillation frequency jitters, the equivalent susceptance B_{eq} must be zero, i.e.,

$$g_{m1} \cong g_{m3} \tag{8}$$

Thus, the sizes of M1 and M3 satisfy $L_3W_1 / L_1W_3 \cong I_{D3} / I_{D1} > 1$.

3. Simulation Results and Implementation

The proposed VCO is implemented in CMOS TSMC 0.18um process. The output power varies from -5.2 to -1.9 dBm and the tuning range is 2.02GHz~2.55GHz (23.1%) when V_{ctrl} varies from 0.6V to 1.8V as depicted in Fig. 3 and Fig. 4, respectively. As shown in Fig. 5, the simulated phase noise is -111dBc/Hz at 1MHz offset. Fig. 6 represents the transient outputs. From the peak times of quadrature 4 output waveforms in Fig. 6, the phase error can be obtained about 5.7 degree. The simulated results of the proposed VCO are listed in Table I where the power consumption is 4.93mW from 0.6V supply voltage and 0.55V bias voltage V_b. The size of the chip is 1.2mm × 1.2mm as shown in Fig. 7.

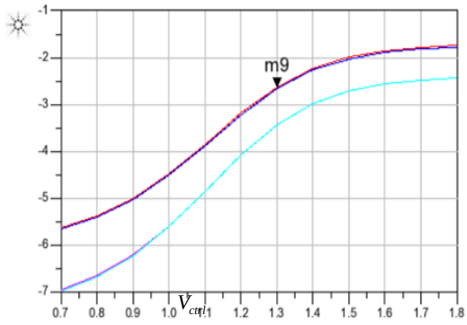

Fig. 3: Simulated output power

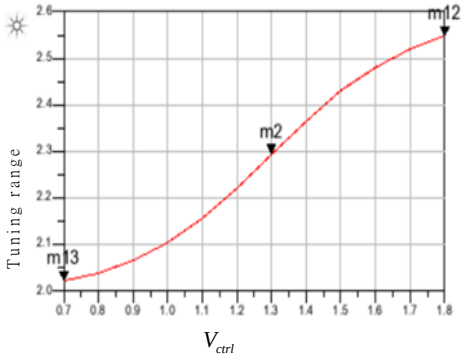

Fig. 4: Simulated tuning range

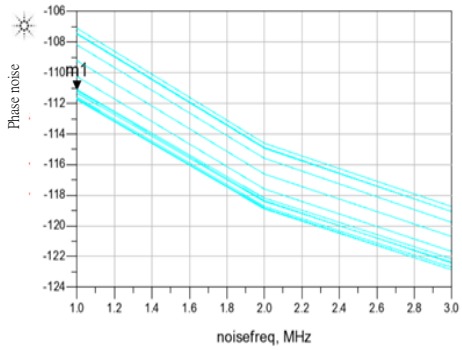

Fig. 5: Simulated phase noise

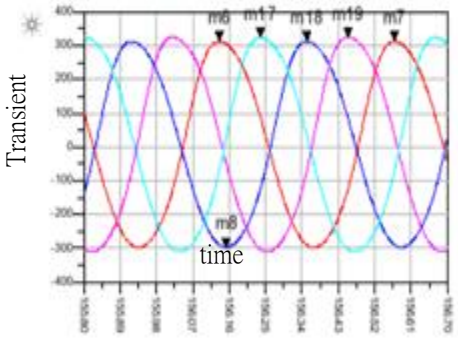

Fig. 6: Simulated output transient

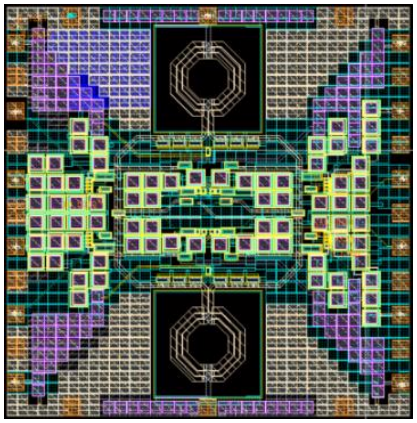

Fig. 7: IC layout

4. Conclusions

In this study, LC-tank QVCO architecture is designed to operate at 2.4GHz with a low supply voltage and low power consumption. This circuit is implemented with the TSMC 0.18 CMOS process. A novel negative resistance is design to oscillate at 4.93mW lower power consumption.

TABLE I Comparison of the Simulated results with the recently published papers about VCOs.

QVCO	This work	[4]	[5]	[6]
Tuning range (GHz)	2.02~2.55	2.41~2.48.	2.40~2.80	2.27~2.65
Phase noise (dBc/MHz)	-111	-109	-124.4	-105
Power consumption	4.93(mW)	9(mW)	15(mW)	5.4(mW)

5. References

[1] S. Hackl, J. Bock, G. Ritzberger," 28 GHz Active I/Q Mixer with Integrated QVCO in SiGe Bipolar Technology", Infineon Technologies AG, Otto-Hahn-Ring 6, D-81730 Munich, Germany, ESSCIRC 2002.

[2] Pietro Andreani, Member, Andrea Bonfanti, Luca Romano, and Carlo Samori," Analysis and Design of a 1.8-GHz CMOS LC Quadrature VCO", IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 37, NO. 12, DECEMBER 2002.

[3] Hye-Ryoung Kim, Seung-Min Oh, Sung-Do Kim*, Young-Sik You* and Sang-Gug Lee,"Low Power Quadrature VCO with the Back Gate Coupling", School of Engineering, Information and Communications University 58-4 Hwaam-dong, Yuseoug-gu, Daejon, 305-732, Korea, Electronics and Telecommunications Research Institute 161 Gajeoug-dong, Yuseong-gu, Daejon, 305-350, Korea.

[4] Dan Lei Yan, Bin Zhao, M.Kumarasamy Raja and Yuan Xiaojun "A 5mA 2.4GHz 2-point modulator with QVCO for Zigbee tranceiver in 0.18-μm CMOS" 2011 International Symposium on Integrated Circuits, 12-14 Dec. 2011

[5] Hechen Wang1 , Feng Zhao1 , Fa Foster Dai1 , Guofu Niu1 , Bogdan Wilamowski1 , Jun Fu2 , Wei Zhou2 , and Yudong Wang2 "A wide tuning triple-band frequency generator MMIC in 0.18μm SiGe BiCMOS technology " Bipolar/BiCMOS Circuits and Technology Meeting (BCTM), 2014 IEEE, 28 Sept.-1 Oct. 2014

[6] Jung-Yu Chang, Chia-Hsin Wu, Shen-Iuan Liu "A Low-Phase-Noise Low-Phase-Error 2.4GHz CMOS Quadrature VCO", Asian Solid-State Circuits Conference, 2005, 1-3 Nov. 2005