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A Broadband Variable Passive True Time Delay at 2-12GHz

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Abstract. A fully integrated passive True Time Delay (TTD) with 66ps continuous changing delay time and less than 11% delay variation has been realized in a TSMC 0.18um CMOS technology. A six-stage trombone configuration is employed to provide 55ps tuning capability with 11ps delay resolution for the coarse tuning part. The fine tuning part employs six LC delay cells with varactor added in both ground branches to provide 11ps continuous delay time. The simulated input and output return loss is better than -10dB over the 2-12GHz range and the insertion loss is -23±1.5dB at 10GHz. The simulated worst-case IIP3 at 6GHz is 1.28dBm and the proposed TTD core occupies 1.782mm^2, respectively.

Keywords: passive, True Time Delay (TTD), CMOS, trombone configuration.

1. Introduction

True time delay (TTD) circuit is a critical block in pulse-based radars and broadband beam forming transceivers which provide flat delay time over a large frequency range [1]. Over the past few decades, various passive and active delay techniques have been explored extensively. MEMS based TTD [2] and Photonic TTD module [3] exhibit large total variable delay, low insertion loss and low delay variation. However, in low cost and integrated systems, these methods are not appropriate. With regard to integrated TTD methods, the RC all-pass filter can offer large variable delay time with only a small chip area [4,5]. However, it is only researched for low frequencies so far. In this paper, the proposed TTD will employ a new structure, which aims to acquire a flat delay response over 2-12GHz with max 11% delay variation.

2. Architecture

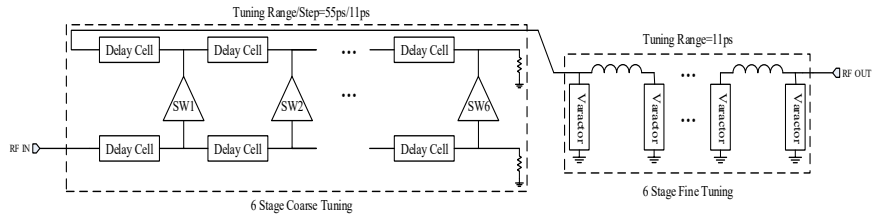

Fig. 1: Block diagram of the proposed TTD circuit

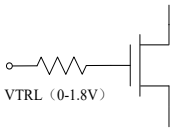

Fig. 2: Implementation of NMOS switches

Fig. 1 shows the basic structure of the proposed TTD circuit. In order to achieve the high tuning resolution and large total variable delay, Coarse tuning part and fine tuning part are combined together [6], which is aimed to achieve 66ps continuous changing delay time over the 2-12GHz range. With six active switches (SW1-SW6) distributed along the input and output delay lines [7], the coarse tuning part provides 55ps delay time with five discrete delay tuning steps of 11ps, respectively. What's more, the fine tuning part, based on varactor mechanisim, provides 11ps continuous variable delay time in total so as to cover the 11ps step of the

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adjacent delay cell of the coarse tuning part. The active switches in this design are implemented with NMOS devices with large series resistor connected to gate to prevent signal leakage shown in Fig.2.

3. Building Block

3.1 Design of the Coarse Tuning Part

The delay cell of the proposed coarse tuning part is shown in Fig. 3a. By cascading multistage delay cells together as shown in Fig. 3b, larger delay time can be obtained. When the cutoff frequency is far greater than the operating frequency, the characteristic impedance Z_0 and the group delay τ of the delay cell are:

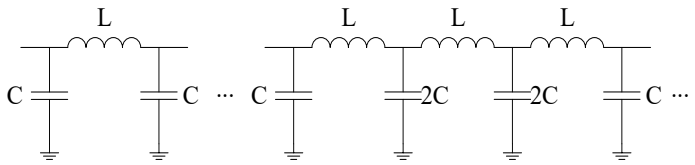

Fig. 3: (a) Delay cell (b) Cascading delay cell

$$Z_0 = \sqrt{L/2C} \tag{1}$$

$$\tau = \sqrt{2LC} \tag{2}$$

The cutoff angular frequency of each delay cell is:

$$W_c = \sqrt{\quad} \quad L \tag{3}$$

Fig. 4 illustrates the delay response of LC delay cell from 1Hz to 30GHz, It can be observed that W_c drops when larger delay time is realized in each delay cell and lead to a larger delay variation at high frequencies. As less delay time in each delay cell contributes to minimizing the delay variation, the proposed TTD circuit adopts a multistage architecture. Each delay cell only provides 1/N of the total delay time by cascading N-stage delay cells. Through this solution, each delay cell's cutoff frequency will be enhanced greatly, and hence, enables a low delay variation at high frequency. However, the more delay stages used in the design, the larger chip area will be employed in practice and hence L is designed to be 225pH, and the capacitance C is 45fF.

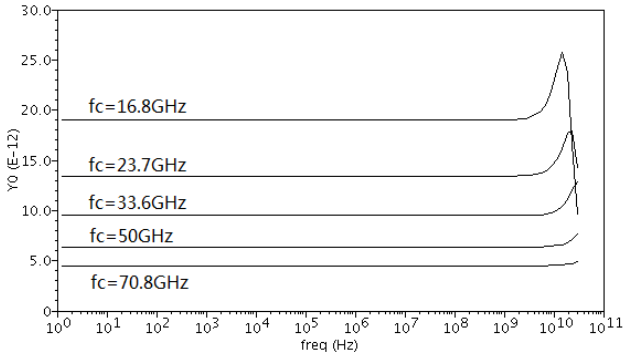

Fig. 4: Delay response of LC delay cell with different cutoff frequencies f_c

3.2 Design of the Fine Tuning Part

Fig. 5 shows the design of six-stage LC fine tuning part. In order to relax the impedance matching between coarse tuning part and fine tuning part, the fine tuning part is needed to have a low characteristic impedance since the coarse Tuning part has a low output impedance. This lead to a large varactor C_{var} and a small inductance L. However, a too large varactor may result in two problems. First, a too large varactor results in large amplitude variation during the fine delay tuning for the insertion loss of the varactor varies as its capacitance changes. What's more, it degrades the fine delay tuning ability because of large parasitic capacitance introduced by the varactor. As a result, L is designed to be 225pH and the varactor ranges from 44fF to 95fF shown in Fig.6. It is worth noting that these parameters in each stage may change a little during the layout implementation because of all kinds of parasitic.

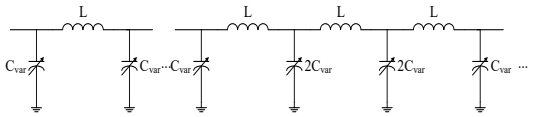

Fig. 5: Design of the fine tuning part

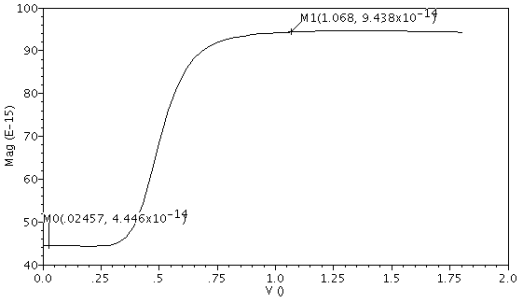

Fig. 6: Varactor characteristic

4. Layout and Simulation Results

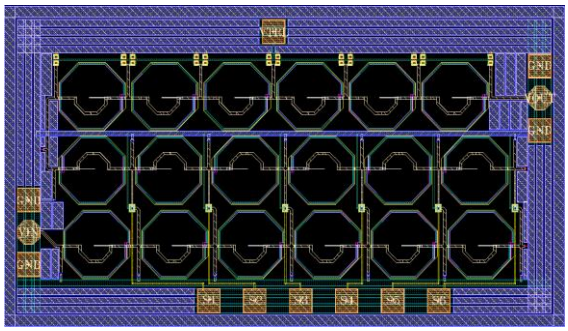

Fig. 7: Layout of the TTD

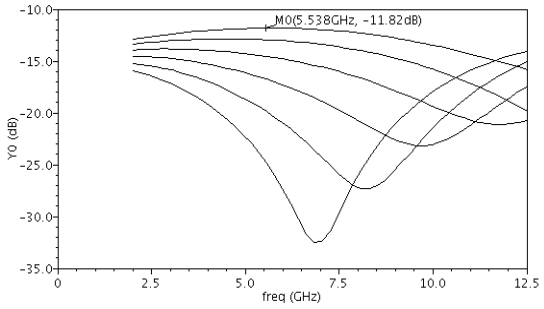

Fig. 8: S11 of the TTD in six states

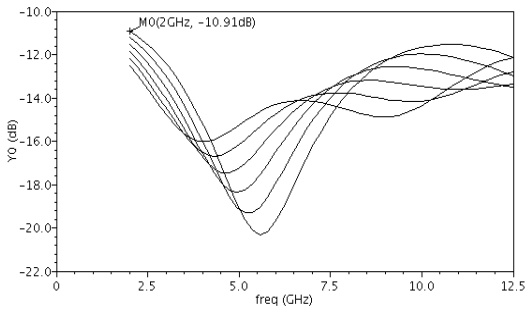

Fig. 9: S22 of the TTD in six states

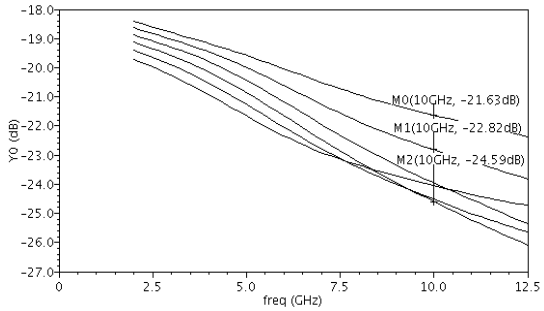

Fig. 10: S21 of the TTD in six states

The fully integrated passive TTD has been realized in a TSMC 0.18um CMOS technology. Fig. 7 shows the layout of the proposed TTD and the chip area is 1.782mm^2. The simulated S parameter are shown in Fig. 8, Fig. 9 and Fig. 10. The S11 and S22 are well below -10dB across the whole simulation frequency of 2-12GHz. The insertion loss of the proposed TTD is -23±1.5dB at 10GHz.

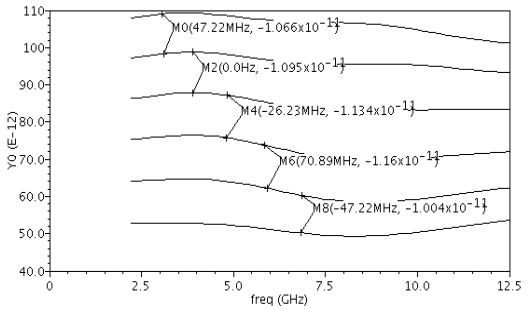

Fig. 11: Group delay of the TTD in six states

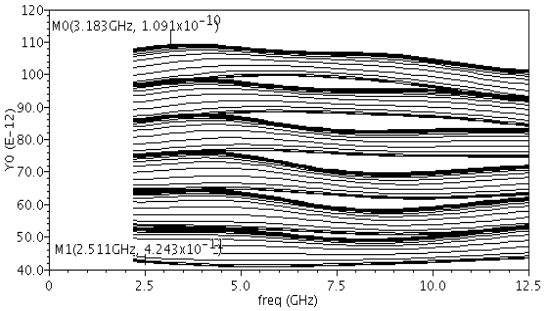

Fig. 12: Group delay of the TTD in all states

Fig. 11 shows the simulated group delay of six states which characterizes how much signal distortion is caused by the TTD. It can be seen that the total achieved changing delay time is 66ps. The group delay of all simulated states is shown in Fig. 12. For phased array antennas, the beam direction is controlled by the relative delay difference between adjacent antennas. The relative phase delay that can be provided by the proposed TTD is shown Fig. 13.

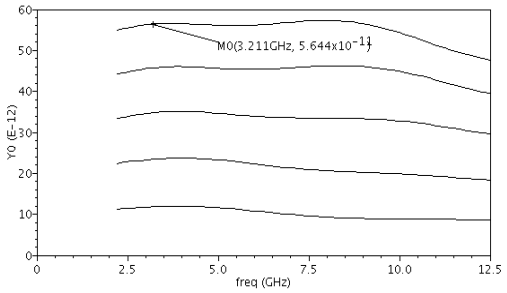

Fig. 13: Relative delay of the TTD in six states

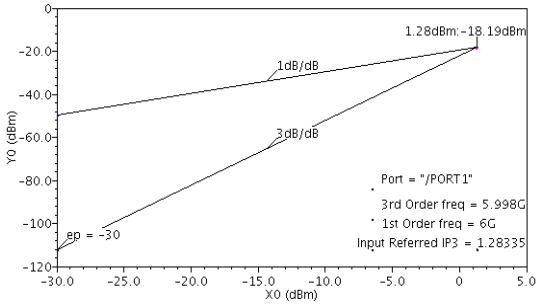

Fig. 14: Worst-case IIP3@6GHz

The simulated worst-case IIP3 is 1.28dBm at 6GHz shown in Fig. 14. Fig. 15 and Fig. 16 gives the simulated time domain delay response. It can be seen that time domain delay response is almost same as group delay. Fig. 17 shows the delay variation of different delay settings which expressed in percentage of the total variable delay time so as to evaluate the flatness of the achieved delay response:

$$\Delta\tau(\%) = \frac{\max(\tau) - \min(\tau)}{\tau_{tot}} \times 100\% \tag{4}$$

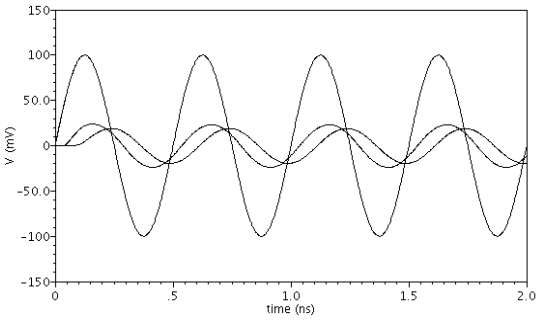

Fig. 15: Time domain delay response@2GHz

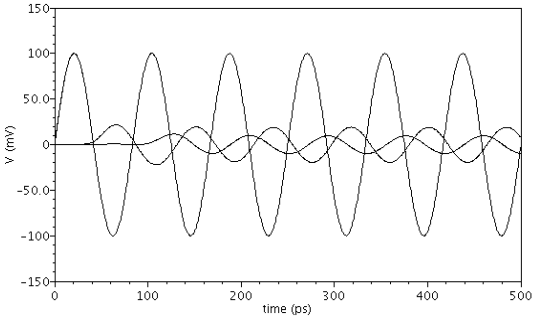

Fig. 16: Time domain delay response@12GHz

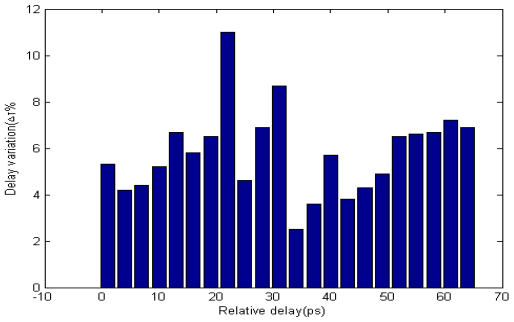

Fig. 17: Delay variation of different delay settings

Table 1: Performance summary of the TTD

Reference	Simulation	EM
Max delay(ps)	66	66
Bandwidth(GHz)	2-12	2-12
Resolution	continuous	continuous
Delay variation	<11%	<11%
S11(dB)	<-10	<-10
S22(dB)	<-10	<-10
S21@10GHz(dB)	-23±1.5	-24±1.5
IIP3@6GHz(dBm)	1.28	1.28
Core area(mm^2)	1.782	1.782

The increasing complexity and operating frequency of a modern microwave circuit make the parasitic effects of interconnects very critical in layout design. Several modeling methods for an interconnect have been introduced. In this paper, the electromagnetic (EM) based approach is employed which is derived from the

numerical solutions of Maxwell's equations that describe the EM behaviors of the physical structures in advance without fabrication at high frequencies. Table I shows the simulated and EM performance of the proposed TTD. It can be seen that the simulated results almost consist with the EM results.

5. Conclusion

A passive broadband TTD circuit with 66ps continuous variable delay time is demonstrated in a TSMC 0.18um CMOS technology. With the proposed matching technique, a flat delay response is achieved from 2GHz to 12GHz with less than 11% delay variation.

6. Acknowledgements

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