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# A 10GS/s 8-bit Current Steering DAC in 65nm CMOS Technology

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**Abstract.** A 10GS/s 8-bit low power current steering DAC in TSMC 65nm CMOS technology is presented. An ingenious way to minimize the mismatch is introduced by mirroring and shifting the current source cells. Also, a switch driver which generates high-cross point and low-swing driving waveform is used in the DAC. It increases the static and dynamic performance of the DAC. The converter adopts the segmented thermometer decoder consisting 4MSBs and 4LSBs, trading off between the complexity and the power. The spurious free dynamic range (SFDR) up to 43dB has been simulated over the entire Nyquist bandwidth at 10GS/s. The total power consumption is 37.5mW at 10GS/s. The DAC occupies an area of 0.7mm × 0.85mm.

**Keywords:** CMOS, current source cells placement, switch driver, thermometer decoder.

## 1. Introduction

In the modern ultra-wide-band wireless communication system, the digital-analog converter (DAC) is critical in signal processing. In high speed communication system, medium resolution DAC with high sampling rate is also used extensively [1-3]. As the development of the modern communication system, the performance of the DAC has become one of the most important bottlenecks. In this paper, a 10GS/s 8-bit current steering DAC is described in TSMC 65nm CMOS technology.

## 2. Architecture

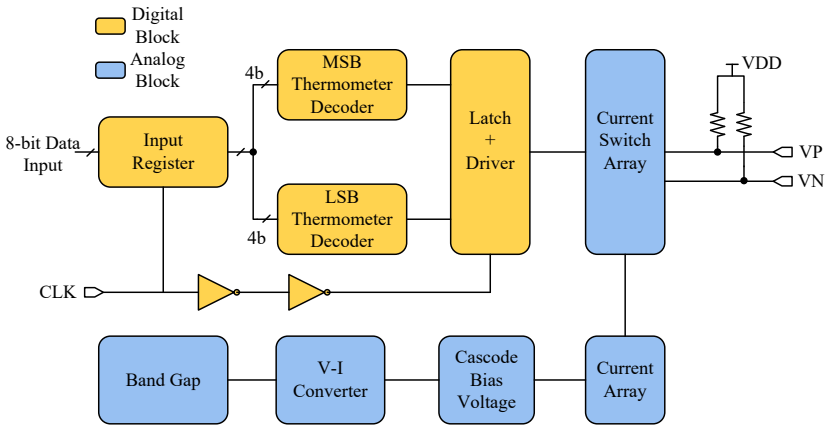


Fig. 1: System diagram of the 8-bit DAC

In high speed DAC design, the current steering architecture is the most suitable, because it can deliver the current to the output resistor directly. Fig. 1 shows the main structure of the DAC. Compromising

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between the complexity and the power, the 4+4 segmentation has been applied. The 4 most significant bits (MSB) are thermometer decoded 15-bit unary code connected to switches. The 4 least significant bits (LSB) are also thermometer decoder, attaining the same delay with MSB decoder and minimizing the output glitch. The switch driver generates the differential signal to control the current cells. The remaining circuit is analog block, the bandgap and the V-I converter provide a stable reference current. By adding a cascode bias voltage circuit, the current flows to the current source array. The switch array controls the direction of the output current. Also for reducing the noise coupling, the analog block and digital block are powered separately.

# 3. Building Block

## 3.1 Current Source Cells

Current source array occupies the most area of analog block because of restrain of static mismatch. Assume two variables, $A_\beta$ and $A_{V_{TH}}$, as the mismatch parameters of the current sources [4]. The relationship between current mismatch parameters and transistor size is presented as follow:

$$WL = \left[ A_\beta^2 + \frac{4A_{V_{TH}}^2}{(V_{GS} - V_{TH})^2} \right] / \left[ 2\left(\frac{\sigma_I}{I}\right)^2 \right] \tag{1}$$

$$\frac{\sigma_I}{I} = \frac{1}{2C\sqrt{2^N}} \tag{2}$$

$$C = inv\_norm_{(-x,x)}\left(0.5 + \frac{Yield}{2}\right) \tag{3}$$

where the $\sigma_I$ is the standard deviation of the current mismatch and the $C$ is the inverse function of the accumulated normal distribution function. The $WL$ and $(V_{GS} - V_{TH})$ represents transistor size and overdrive voltage respectively. It can be calculated the size of the current source for the static match requirements. In normal situation, for the INL yield up to 99.7%, the $C$ is about 3.2. To achieve better match, it can set bigger $N$. With the designed current and overdrive voltage, the size can be got simultaneously.

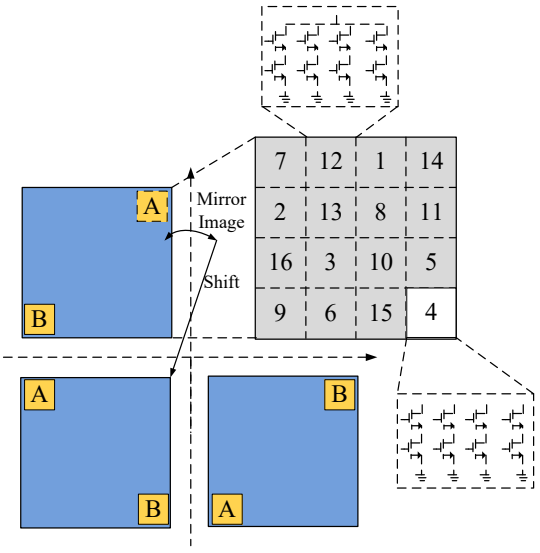


Fig. 2: Current source cells assignment

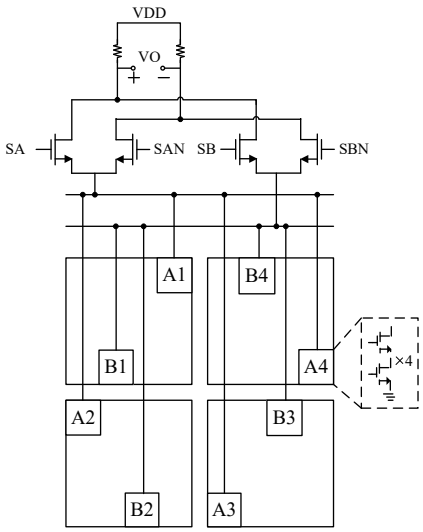


Fig.3: Specific connection of current source cells

There are 255 current sources in total, so the mismatch is a big problem. Many references introduce innovative way to reduce the graded and symmetrical errors of the cell array in layout design. Fig.2 describes one specific assignment. The cells are placed respective positions in a predetermined selection sequence, for example, to a so called “magic square”. Each MSB cell has 4 current sources connected in parallel. The 15×4 MSB sources are placed in 4 concentric symmetrical quadrants. It just mirrors and shifts the current source cells from one quadrant to the closed quadrant except the number 4 and 7 as shown in below, as the 15 LSB sources which placed in number 4 are assigned in the center of the array to minimize the glitch. The assigned

ordinal positions are such as to tend to equalize the respective sequence-position sums for different rows and columns of the array, where the sequence-position sum for a row or column is determined by summing the respective ordinal positions of the cells in the row or column concerned [5]. The sequence of the cells is just as the magic square. Each quadrant has 4×4 numbered cells and shares the same order number over 4 cubes. Fig.3 gives the specific connection of current source cells.

## 3.2 Switch driver

To minimize the influence of the current source mismatch, the current cells occupy the most area of the analog block. The massive size leading to large parasitic effect at the source of differential switches makes it necessary to minimize the glitch at the source, because strong glitch will drastically decrease the SFDR of the output signal. So, it's necessary to minimize the size of the switch to reduce the parasitic effect.

In the design of the DAC, many MOST switches will be used, so the clock feed through effect is an inevitable problem. As shown in Fig. 4, the $C_{GS}$ and $C_{GD}$ are the coupling capacitor from the gate to the source and the drain. The driver signal of the gate can transmit to the input and output through the coupling capacitor. The $C_L$ is the load capacitor, the $\Delta V_{clk}$ is the swing of the driver signal. The output signal is as bellow:

$$\Delta V_{out} \approx \frac{C_{GD}}{C_L + C_{GD}} \Delta V_{clk} \tag{4}$$

As indicated by the formula, a change in the clock signal causes an instantaneous change in the output signal, it will emerge a strong glitch at the output of the DAC. Of course, one effective solution is to generate high-cross point and low-swing driving waveform [6]. The high-cross differential signal can minimize the switch time from open to close, and the differential switch transistors won't be shut down at the same time, thus increase the speed of the current steer and reduce the glitch. The smaller fluctuation of the source, the better output wave. The low-swing will reduce the leakage to the source, thus decrease the effect of the clock feed through, so the output current source will be accurate at the same time.

This paper presents one simple structure in Fig. 5. The D and DN are the input symmetrical differential signal, the S and SN are the drive signals for differential switches, and the output swing is between VDD and the designed low voltage, VREF. The size of M1 and M4 is same, the M2 and M3 share the same size too. By enlarging the size of M1 and M4, it can accelerate the rising speed, similarly, by reducing the size of M2 and M3, it can slow the falling speed. So, the high-cross point and low-swing differential signal can be achieved. Fig.6 shows the simulation result.

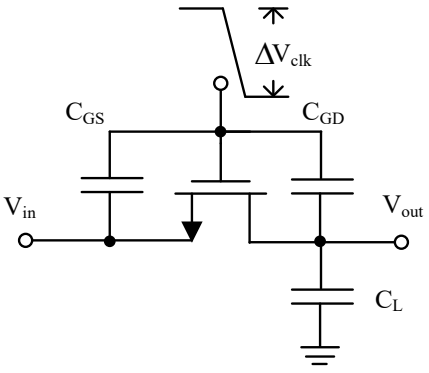


Fig. 4: Clock feed through model of the switch

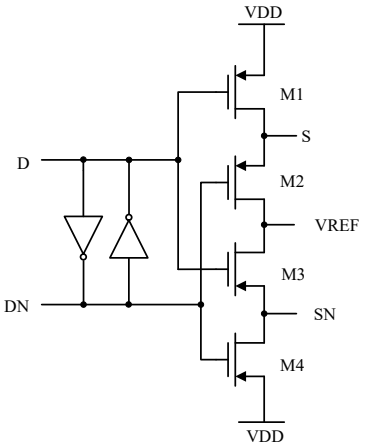


Fig. 5: Switch driver

## 3.3 Thermometer Decoder

As shown in Fig.1, this design adopts 4+4 all thermometer decoder, and the 4-bit decoder is the most important part. It often decides the speed of the signal rate of the DAC. Fig.7 describes the specific structure of the thermometer decoder. The thermometer decoder adopts the row-column decoder, and the higher two bits are used the row decoder, and the lower two bits are used the column decoder. As shown in the Fig.7, the

code 1010 means ten high level output in total. Many logic units will connect with the first stage, it means a big parasitic capacitance on it, so a driver is added to reduce the influence of the capacitance. According to [7], if the differential switch driver signals are not synchronous, the SFDR of the output signal will significantly decrease, so the trigger is used to synchronize the output signal.

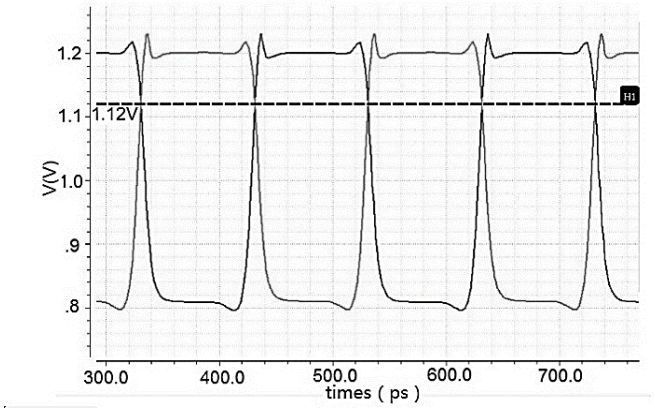


Fig. 6: Output of the S and SN

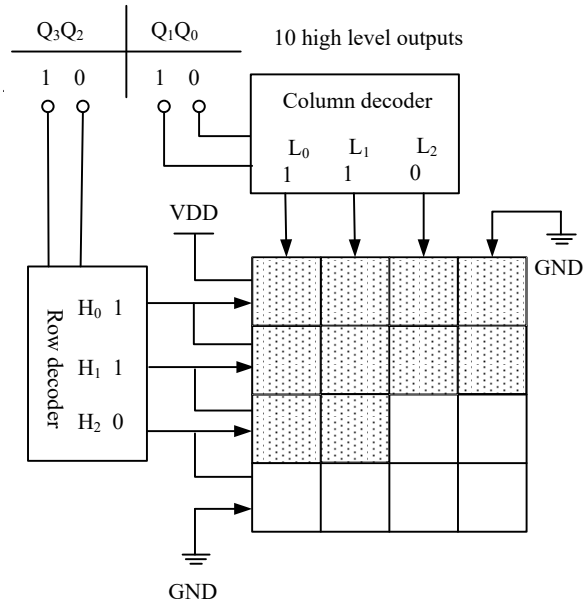


Fig. 7: Structure of the thermometer decoder

## 4. Layout and Simulation Results

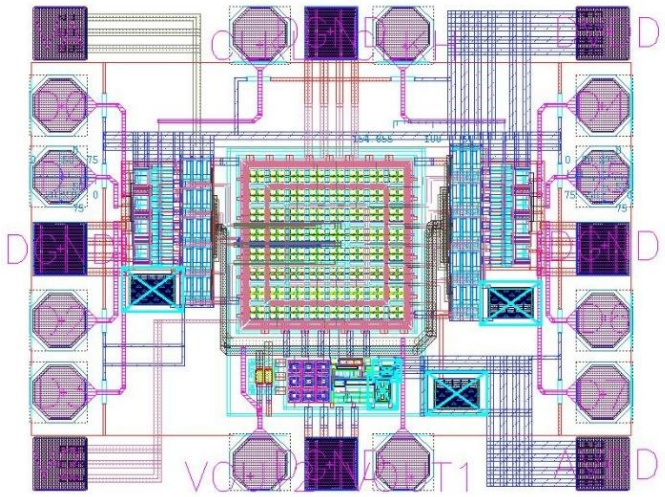

Fig. 8: Layout of the DAC

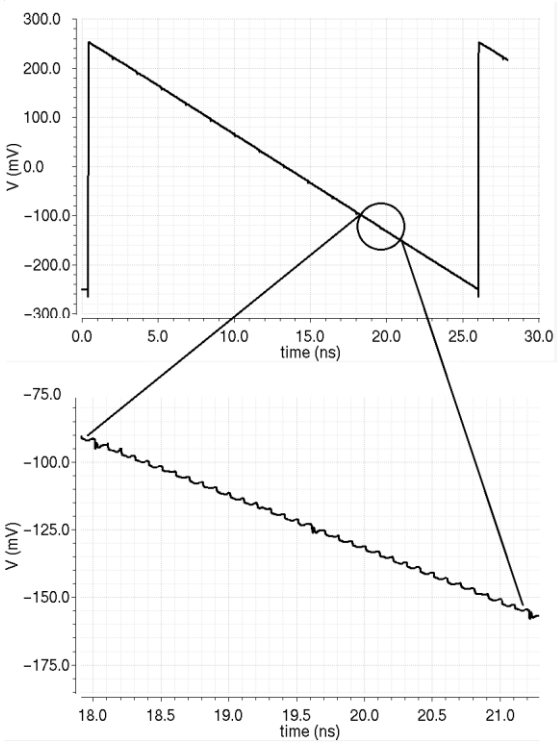


Fig. 9: Step waveform of differential output

The layout of the 8-bit DAC is shown in Fig. 8. Fig. 9 presents the step waveform when the input code decreases from 11111111 to 00000000 with the sampling rate up to 10Gb/s. The DNL, INL results are described in Fig. 10. It is obvious that the static requirement is satisfied with both DNL and INL less than 0.5LSB. The dynamic performance is simulated with Nyquist bandwidth at 10GS/s. The SFDR results is presented in Fig.11. With the high-cross point and low-swing driving signal, the SFDR is up to 43dB during

the Nyquist bandwidth.

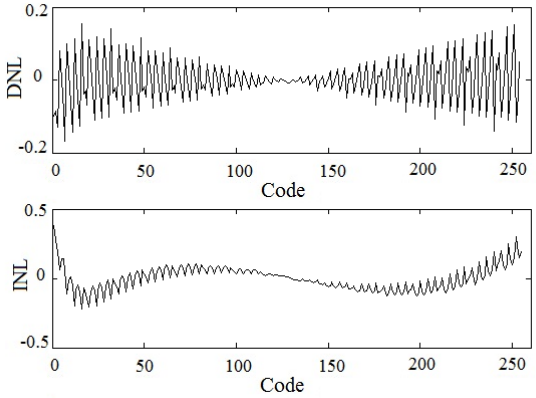


Fig. 10: Results of the DNL and INL

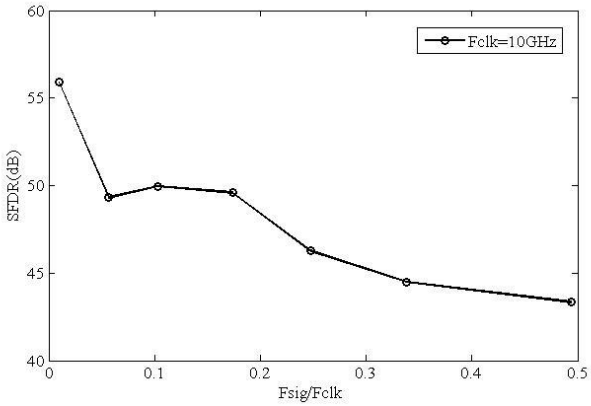


Fig. 11: SFDR result of the 8-bit DAC

## 5. Conclusion

This paper presented an 8-bit 10GS/s current steering DAC. The DAC shows the good static and dynamic performance because of the ingenious placement of the current sources and the high-cross point and low-swing driving signal. The DNL is less than 0.2LSB and the INL is less than 0.5LSB. The SFDR is better than 43dB over the entire Nyquist bandwidth. The power consumption is 37.5mW. The DAC is presented in 65nm CMOS technology and occupies 0.595mm$^2$.

## 6. Acknowledgements

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