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# Design of a Chaotic Signal Generator with Initial Value Tuning via the Pulse-Width Control Circuit

Chang-Hsi Wu[+1], Hao-We Chen[2], Yuan-Long Wu[3] and Cheng-Hsiung Yang[4]

[1,2]Longhua University of Science and Technology
[3,4]National Taiwan University of Science and Technology

**Abstract.** In this paper, chip designs of chaotic signal generator (CSG) with initial value tuning are proposed. The initial value that can uniquely decide the waveform from CSG is adjusted via the pulse-width control circuit (PWCC). With the initial value controlled technique, the CSG can be used as the modulator for encryption and decryption applications. The PWCC chip occupies area of $1.05\times1.08$ $mm^2$ in $0.18\mu m$ CMOS process with power dissipation of 55.72mW from a 3.3V supply voltage, while the CSG chip occupies area of $0.959\times0.77$ $mm^2$ in $0.35\mu m$ CMOS process with power dissipation of 475mW from a 3.3V supply voltage.

**Keywords:** chaotic signal generator, initial value tuning, pulse-width control, encryption and decryption , CMOS process.

## 1. Introduction

Chaotic systems provide a variety mechanism for signal design and generation, with valuable applications to communications and signal processing. Because chaotic signals are typically broadband, noise-like, and difficult to predict, they can be used in the message science for masking information or bearing waveforms. They can also be used as modulating waveforms in spread spectrum systems. This can be useful in many practical circumstances like securing communication channels [1-3], masking signals [4-6], spreading data sequence, or for generating random signals [7]. Thus, Chaotic oscillator is a key block in building an encrypted communication.

In this paper, we proposed two chip designs. One is a PWCC which is used to tune the initial value of chaotic signal and the other is a CSG of four-dimensional modified Lorenz-Stenflo system. In the designed PWCC, the width of input pulse signal generated by a push-type non-stage switch can be widened and adjusted via a tunable current source. The CSG is implemented by two multipliers and four non-inverting weighted addition integrators; they are corresponding to a four-dimensional Lorenz-Stenflo characteristic [8-9].

## 2. Design Principle of the Circuit

The proposed CSG circuit with initial value tuning via a PWCC is shown in Figure 1. The design principle of this architecture is illustrated as following three parts.

### 2.1. Chaotic signal generator:

The modified Lorenz-Stenflo system in Figure 1 [10] constructed by two multipliers and four non-inverting weighted addition integrators is used to produce chaotic signals of the form in equation (1). In this

[+] Corresponding author. Tel.: + 886-919534070; fax: +886-28209-5165.
*E-mail address: cswu88@gmail.com.*

design, the values of $R_1 \sim R_{10}$ and $C_1 \sim C_4$ are appropriately selected to specify the parameters of a=3.7, b=1.5, c=26 and d=0.7 which can induce a chaotic signal.

$$\begin{aligned} \dot{x}_1 &= ax_2 - ax_1 \\ \dot{x}_2 &= cx_1 - x_1x_3 \\ \dot{x}_3 &= x_1x_2 - dx_3 \\ \dot{x}_4 &= -bx_1 - ax_4 \end{aligned} \tag{1}$$

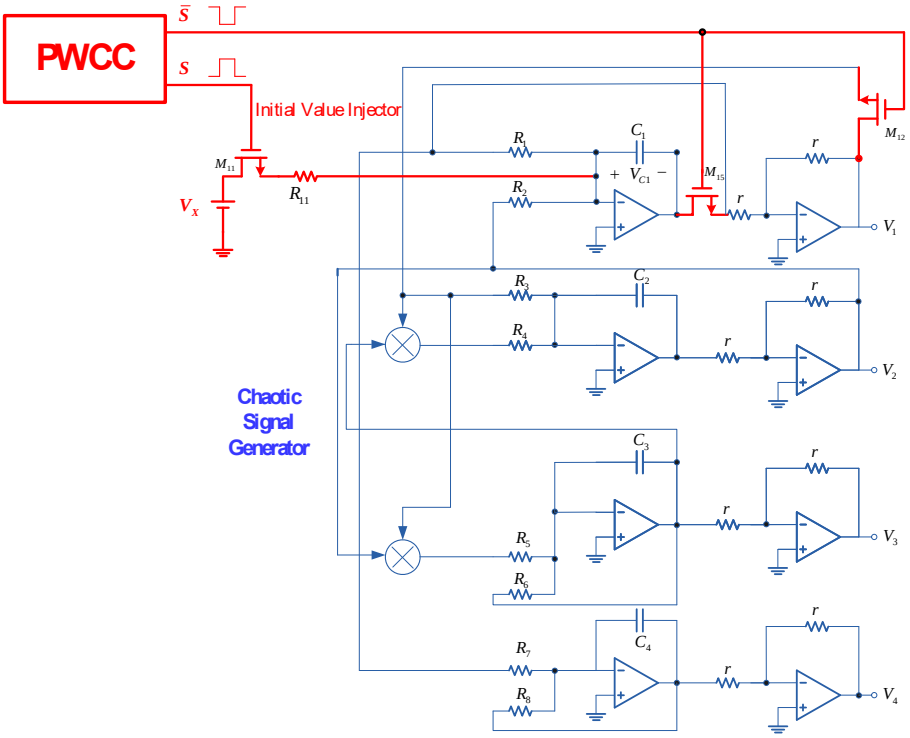



Fig. 1: The proposed CSG circuit with initial value Tuning via a PWCC

## 2.2. Initial value injector:

Since each signal uniquely corresponds to one initial value, the initial value can be adjusted by injecting a constant current into the capacitor $C_1$ in Fig 1 for a period of time to obtain different chaotic signals. After finishing charge of initial value, the chaos is immediately started up, the transistor $M_{11}$ will turn off and transistors $M_{12}$ and $M_{15}$ will turn on, and the initial value of $C_1$ is

$$V_{C1}(0) = \frac{V_X}{R_{11}C_1}T_P \tag{2}$$

where $T_P$ is the output pulse width of the PWCC. From equation (2), the initial value of CSG is larger when the pulse width of PWCC is wider.

## 2.3. Pulse-width control circuit:

The PWCC is shown in Fig. 2 [11]. When the input $v_I$ is rising to high, the output $v_{O1}$ of the first (NOR) gate and the input $v_{I2}$ of the second (NOT) gate are both pulled-down to low (0V) due to continuity of $V_{C5}$. Then the output $\phi$ of PWCC is pulled-up to high ($V_{DD}$). In this situation, the current mirror constructed of M1, M2 and M3 pushes a constant current $I_R$ into the capacitor C5 and the voltage $v_{I2}$ starting to rise. At the trigger beginning, even if the input $v_I$ goes to low, the output $v_{O1}$ of the first gate still remains 0V because lower $v_{I2}$ makes the output $v_{O2}$ of the second gate remains high. As the waveforms depicted in Fig. 3, the output $v_{O2}$ turns to low (0V) only when $v_{I2} \geq V_{th} = V_{DD}/2$. Thus the resulting output pulse-width can be obtained as

$$T_P = \frac{V_{th} - V_{OL}}{I_R}C_5 = \frac{V_{DD}}{2I_R}C_5 \tag{3}$$

It can be seen from equations (2) and (3) that the initial value of CSG can be increased by reducing the current $I_R$. Based on the above principles, the current $I_R$ can be controlled by the digital signals $V_{b1}, V_{b2} \sim V_{b16}$ in PWCC as shown in Figure 2.

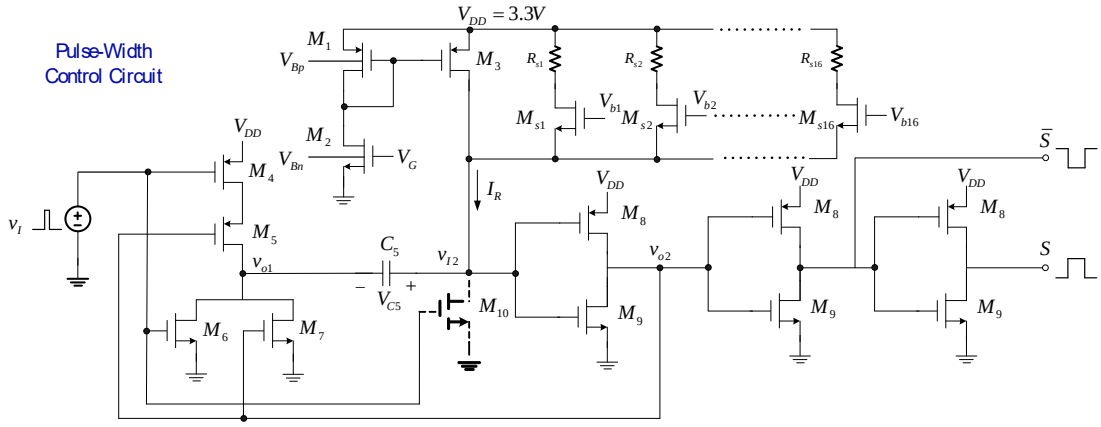



Fig. 2: The proposed PWCC

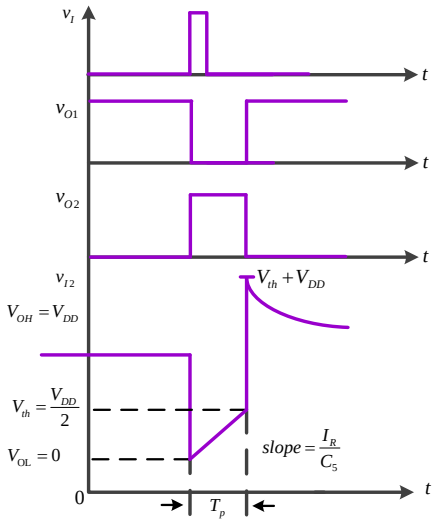



Fig. 3: Waveforms in the proposed PWCC

## 3. Simulation and Implementation

The electrical performances of the designed CSG chip and PWCC chip are presented in Table I and Table II, respectively. Figure 4 to Figure 6 depict the simulated output pulse widths of the PWCC and two dimensional phase portraits of the designed CSG for the corresponding initial values of 0.1, 0.3 and 0.5 volt, respectively. The Micro-photographs of CSG and PWCC chips are represented in Figure 7 and Figure 8, respectively.

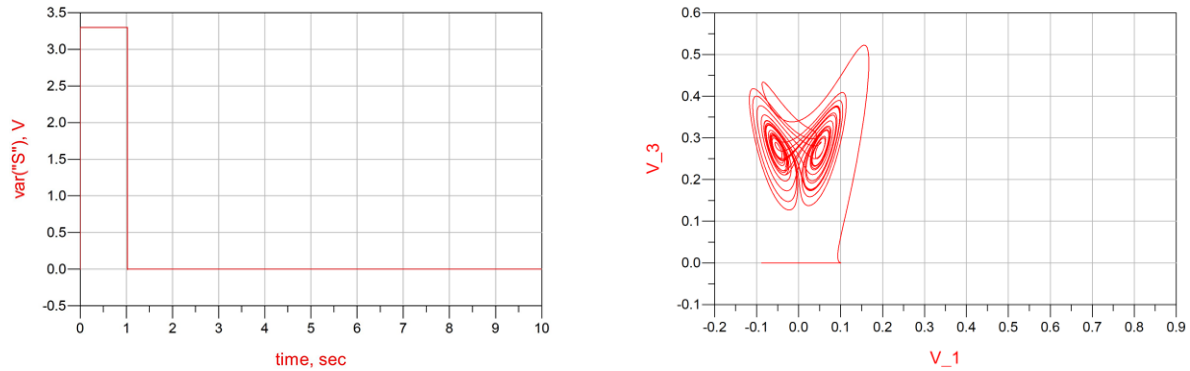



Fig. 4: The simulated pulse width and two dimensional phase portrait for the initial value of 0.1 volt.

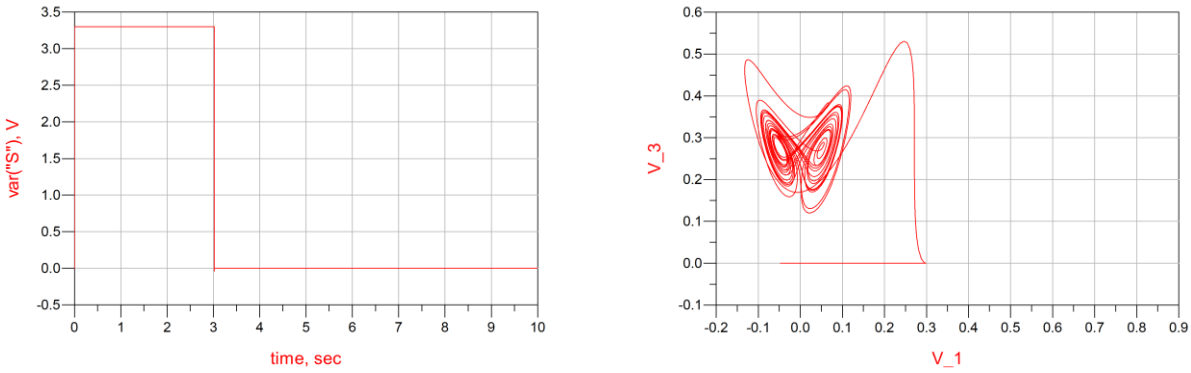



Fig. 5: The simulated pulse width and two dimensional phase portrait for the initial value of 0.3 volt.

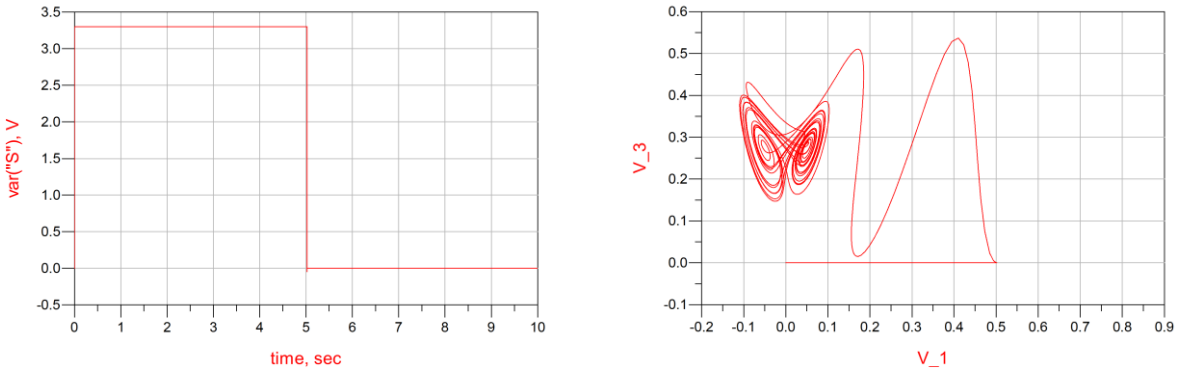



Fig. 6: The simulated pulse width and two dimensional phase portrait for the initial value of 0.5 volt.

# 4. Conclusions

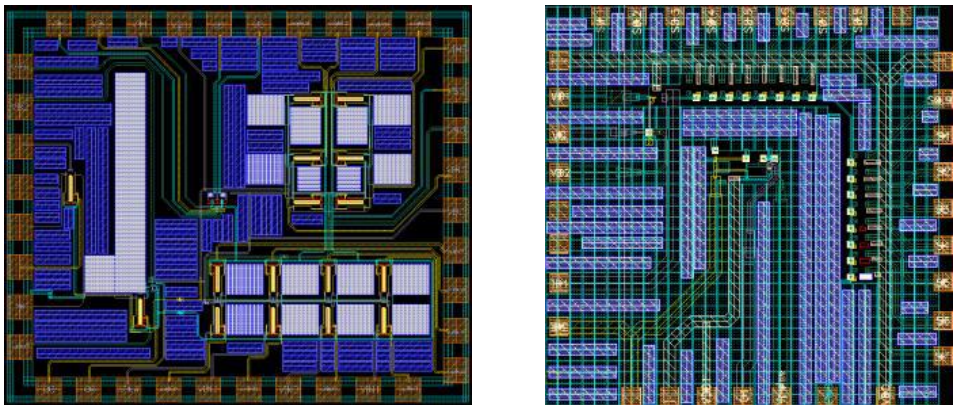
In summary, the proposed chaotic signal generator with initial value tuning has the characteristic of waveforms dependent of the initial values. The circuit design is divided into two parts. One is the pulse-width control circuit chip and the other is chaotic signal generator chip. The PWCC chip occupies area of 1.05×1.08 $mm^2$ in 0.18$\mu$m CMOS process with power dissipation of 55.72mW from a 3.3V supply voltage, while the CSG chip occupies area of 0.959×0.77 $mm^2$ in 0.35$\mu$m CMOS process with power dissipation of 475mW from a 3.3V supply voltage.

Tab I: The electrical performances of the designed CSG chip

| | |
|---|---|
| Technology | TSMC 0.35μm CMOS |
| Chip Size | 0.959×0.77 $mm^2$ |
| Power Dissipation | 475mW |

Tab. II: The electrical performances of the designed PWCC chip

| | |
|---|---|
| Technology | TSMC 0.18μm CMOS |
| Chip Size | 1.05×1.08 $mm^2$ |
| Power Dissipation | 55.72mW |



(a) (b)

Fig. 6: The micro-photographs (a) the CSG chip and (b) the PWCC chip.

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