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A Portable High-Speed Data Acquisition System Based on AVR and CPLD

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Abstract. A portable storage-type data acquisition system based on ATmega162 (AVR) Micro Controller Unit and CPLD is proposed by this research. The features of proposed system are low cost, high speed, high reliability, portable, easy to implement. This paper describes the hardware circuit principle and the main control program of the data acquisition system. According to analyze the characteristics and conversion timing of MAX1308 ADC, the ADC circuit and its peripheral circuits are proposed. The entire system timing state is controlled by the program of AVR and CPLD. The experimental result shows that the designed system can achieve the original design requirement. The Multi-channel acquisition speed is greater than 10MB / s.

Keywords: Multi-channel acquisition, Pipeline Storage, AVR, CPLD, NandFlash.

1. Introduction

Most of the input system information is analog. In order that the computer can handle these analog values, the data acquisition system must convert the analog into the digital. CPLD were developed on the basis of PAL, GAL and other logic devices [2], [3]. The CPLD is suitable for timing logic circuit, combination logic circuit and other logic circuit application. The high integration capacity of CPLD greatly reduces the circuit board size and the system cost and improves system performance and reliability.

There is a storage part in a molded detection system. No matter electrical signals, optical signals, sound signals, magnetic signals, etc. are received and converted into digital signal by the detector .The system will pass the digital signal to the processor to complete the analysis. For high-speed acquisition and storage systems, it is often necessary to purchase expensive high-speed acquisition cards and other equipment. Based on CPLD and AVR [4] this paper designs a low-cost, high-speed acquisition and storage hardware system.

2. Overall Design Scheme

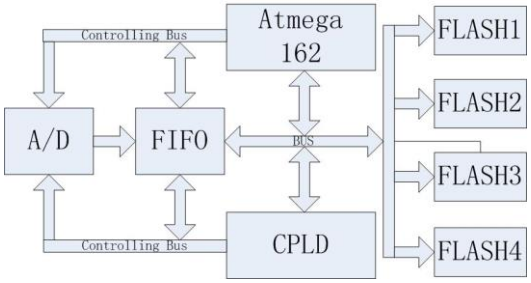

Fig. 1: System design principle diagram

The proposed system uses an ATmega162 microcontroller as the main controller. The CPLD is used to generate control timing. The both are coordinated to carry out data collection and transmission control.

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Figure 1 shows a block diagram of the overall design of the system. The data acquisition system [5] works as follows: the physical quantity is converted to the analog voltage value after passing through the sensor. The ADC converts the analog voltage value to the digital. These digital quantities will then be transferred for storage and processing. In this system, the acquired analog signal is converted to the digital by A/D device through the control of CPLD and AVR. The conversion result is buffered into a First-in-First-out buffer chip (FIFO) and then transferred to nonvolatile NandFlash array. The FIFO not only can achieve the cache function, but also can solve the contradictions which the number of the A/D conversion data bits differ from the number of data bits in the NandFlash memory.

3. Module Design：

3.1. Acquisition Module

The data acquisition system consists of acquisition module, control module and storage module. The system uses a MAX1308 as the A/D chip which has 8-channels programmable configuration. It can accept digital inputs to activate each channel separately. Its conversion time is different when the number of selected sampling channels is different. Other features include 20MHz T/H input bandwidth and have internal clock, and low power consumption and so on.

3.2. Control and Storage Module

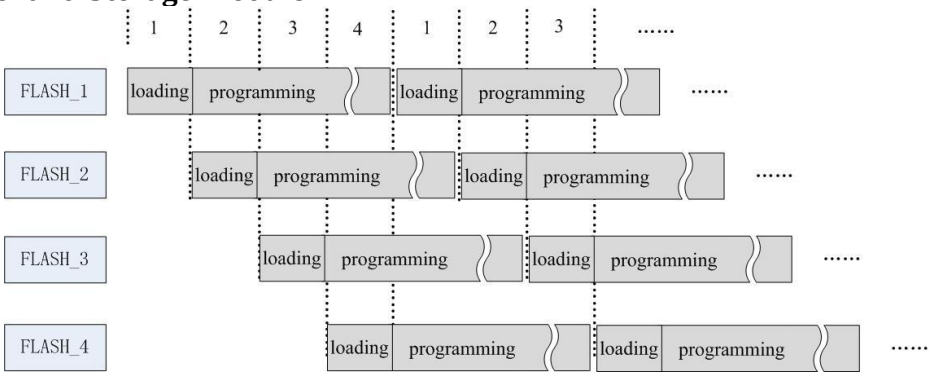

Fig. 2: Pipeline operation module with four groups of NandFlash

Due to some inherent characteristics of the NandFlash, the new data from the the I/O port can be loaded to its cache plane after the previous data in the cache plane is solidified into the internal storage unit of the NandFlash. Writing to the NandFlash memory requires both the data loading phase and the programming phase. The data loading phase writes data to the page data register which is the cache plane of the NandFlash via the I/O port. The programming phase transfer data from the page data register to nonvolatile memory cells inside the chip. The data programming phase is automatic and does not require the other external operations, but it takes a long time. Its typical value is 200 microseconds. The main disadvantage of single NandFlash storage system is that the data collected by A/D cannot be loaded uninterruptedly. To cope with this problem, we introduce a pipeline storage method, as shown in Fig.2. First of all, the first Nandflash loads data. After the data is loaded, the first NandFlash enter the automatic data programming phase and the second NandFlash load data in the same time. After the data is loaded, the second NandFlash enter the automatic data programming phase too. The same processes are performed as above for the third NandFlash and the fourth NandFlash. After the data of the fourth of NandFlash is loaded, the first NandFlash just completes the automatic programming phase. And then from the first NandFlash to the fourth NandFlash the loading data phase and the automatic programming data phase are performed repeatedly. The above operations are done in this way until the data acquisition is completed.

For single piece of NandFlash, the data loading phase is implemented after the completion of the programming phase, repeatedly. The four groups NandFlash memory pipeline works as shown in Figure 2. On the entire system point of view, for the memory system composed of four pieces of NandFlash memory，the data loading phase is always being implemented to store data. This can ensure that the data is stored uninterruptedly into NandFlash and the storage speed is greater than the acquisition speed, which can

prevent the data from being lost in the storage process due to the slow speed and storing data intermittently in the single piece of NandFlash memory system.

4. The Design and Implementation of the Program

4.1. Acquisition Module Implementation

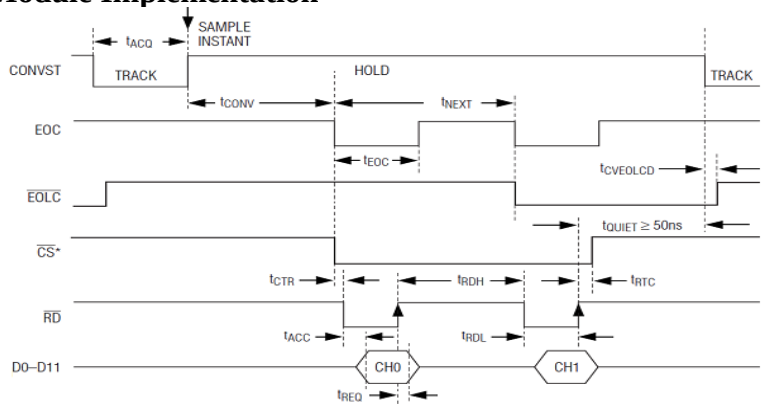

Fig. 3: The conversion process in the read operation - Selecting channel 3 and channel 7 (internal clock)

The acquisition section is implemented in this part. In the acquisition section, when the A/D to collect data, the required control timing diagram are shown in Figure 3. In the figure 3, both the 0th and 1th channel are selected for analysis. When the control signal CONVST is low, the control pin is active and the acquisition function is triggered. When the conversion is complete, the EOC pin level is low. The CS signal goes low after waiting for the t_{CTR}. The RD read signal can be started. After waiting for t_{ACC} time, 12-bit data will appear on the data output pin D0-D11 pin. At this time, The FIFO can read the results of A/D conversion. After waiting for the t_{RDH}, the 1th channel data can also be read. In this way, a single A/D data acquisition process is complete. The whole process is to repeat the above process. According to the requirements of the A/D timing diagram in Figure 3, a state machine controlling A/D conversion is designed. The conversion diagram of the state machine designed to control A/D conversion is shown in Figure 4.

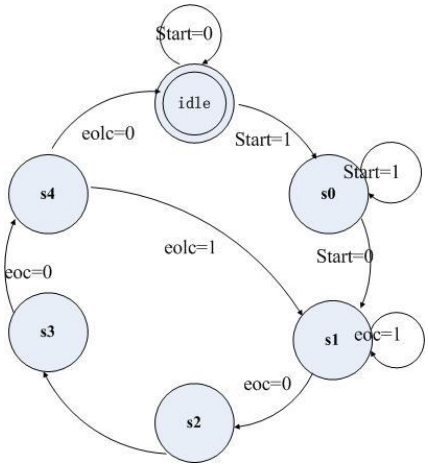

Fig. 4: The state machine to control A/D conversion

Some of the main VHDL program codes of the state machine controlling A/D conversion are as follows:

```
u2: process (clk_32M,next_state,start)
begin
 if(start='1')then
   present_state <= s0;
elsif(clk_32M'event and clk_32M='1') then
   present_state <= next_state;
end if;
```

end process u2;

The program is downloaded to the CPLD for running and debugging. After the circuit debugging and testing， the oscilloscope timing waveform generated by the state machine for Controlling of 8-channel A/D simultaneous conversion is shown in Figure 5. The 0th, 1th, 2th, 3th, 4th in Fig. 5 correspond to CONVST, EOC, EOLC, CS, RD in Fig 3, respectively. The 5th channel is the signal to write data to the FIFO. From the screen of the oscilloscope，it can be found that 8 consecutive pulses fully meet the timing requirements required in Figure 3.Using the system design of the acquisition program can achieve multi-channel simultaneous acquisition requirements. According to the collected pulse width analysis, it can be seen to meet the acquisition speed of 10Mb/s design requirements.

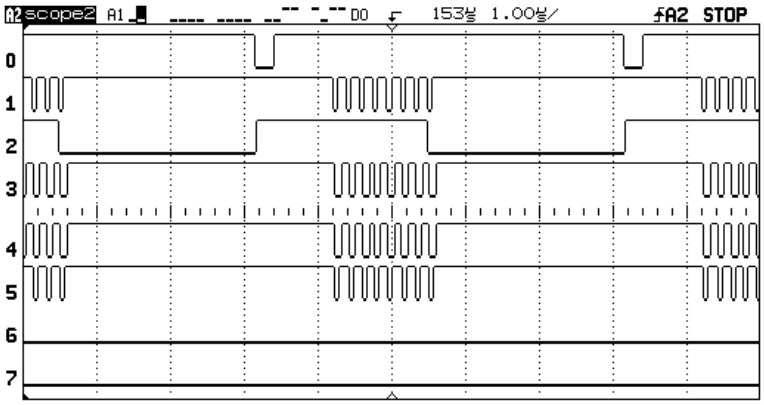

Fig. 5: Oscilloscope waveform of the state machine to control A/D conversion

4.2. The Implementation of the Storage Module

The storage section is implemented in this part. During the data loading phase, the system uses the Direct Memory Access (DMA) method to transfer data. The DMA controller is generated by the CPLD.

Some VHDL program is as follows:

```
FLASH_NUM=1;
    cmd_flash_ce(0x00); //flash_ce
            STATUS_RB();
     NF_cmd(Read_status);
            c=*FlashRD &0x01;
            NF_cmd(Program_cmd);
NF_addr(DMA_addr[0],DMA_addr[1],DMA_addr[2],DMA_addr[3],DMA_addr[4]);
```

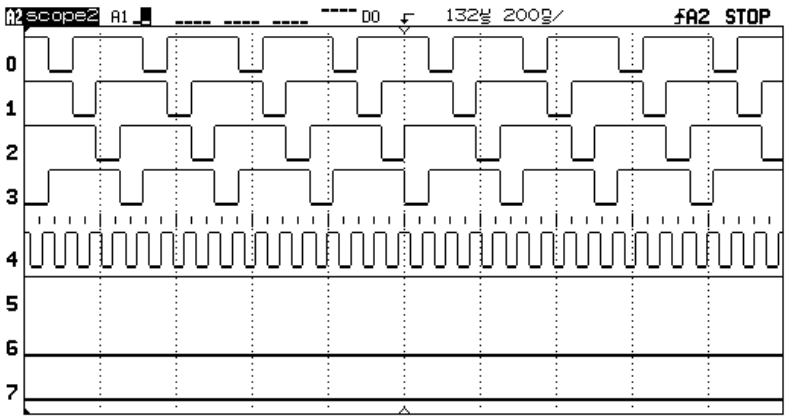

Fig. 6: Oscilloscope waveform of writing data to the NandFlash

When the FIFO half full flag signal HF generates an active level, the ATmega162 initiates an interrupt. During the interrupt routine, the ATmega162 generate the controlling command and the effective address, and start the DMA controller. Once the DMA controller is started, the ATmega162 will not control the data

bus and address bus. The ATmega162 go to the background for efficient address calculation and allocation. The DMA controller takes over the data bus and the address bus and participates in the data transfer process. The entire process transferring data from FIFO to NandFlash memory is controlled by the DMA controller. A page of 2048 bytes of data are transferred once starting a DMA process. During an interrupt, the 16K bytes of data will be transferred, which is determined by the capacity of the FIFO. The oscilloscope timing diagram is shown in Figure 6: the 0th, 1th, 2th, 3th channel is the timing waveform reading data from FIFO. And the 4th channel is the timing waveform writing data to NandFlash.

5. Conclusion

By the combination of AVR and CPLD, a portable high-speed data acquisition and storage system with low cost is designed. Based on the analysis of the characteristics of MAX1308 analog-to-digital converter and the timing of control, the ADC and its peripheral circuits are designed. In the storage section, the collected data is stored by the proposed pipeline way which uses four groups of NandFlash memory chips. Programming with VHDL language In the CPLD，respectively, implement the acquisition module, DMA controller module and the writing/reading NandFlash memory module. After the completion of the entire system debugging, the test result shows that the performance of the acquisition system is stable, the acquisition speed in parallel conditions can be maintained at 10Mb/s or more. The design of the system is in line with the intended design requirements. In the future, the A/D in this paper can be replaced by a high-speed A/D, in order to increase the acquisition speed of the data acquisition system. In order to increase the storage speed of the data acquisition system，the number of each group NandFlash will be increased to achieve a parallel storage, which can multiply increase the storing speed of the data storage system. Theoretically, the way of the pipelined and parallel storage can increase the data real-time storage speed to hundreds of MBytes or a few GBytes per second or more.

6. Acknowledgements

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